

Cedar Schematic Beema

2014-03-05

REV : A00

DY : None Installed

UMA: UMA only installed

OPS: DISCRTE SG installed

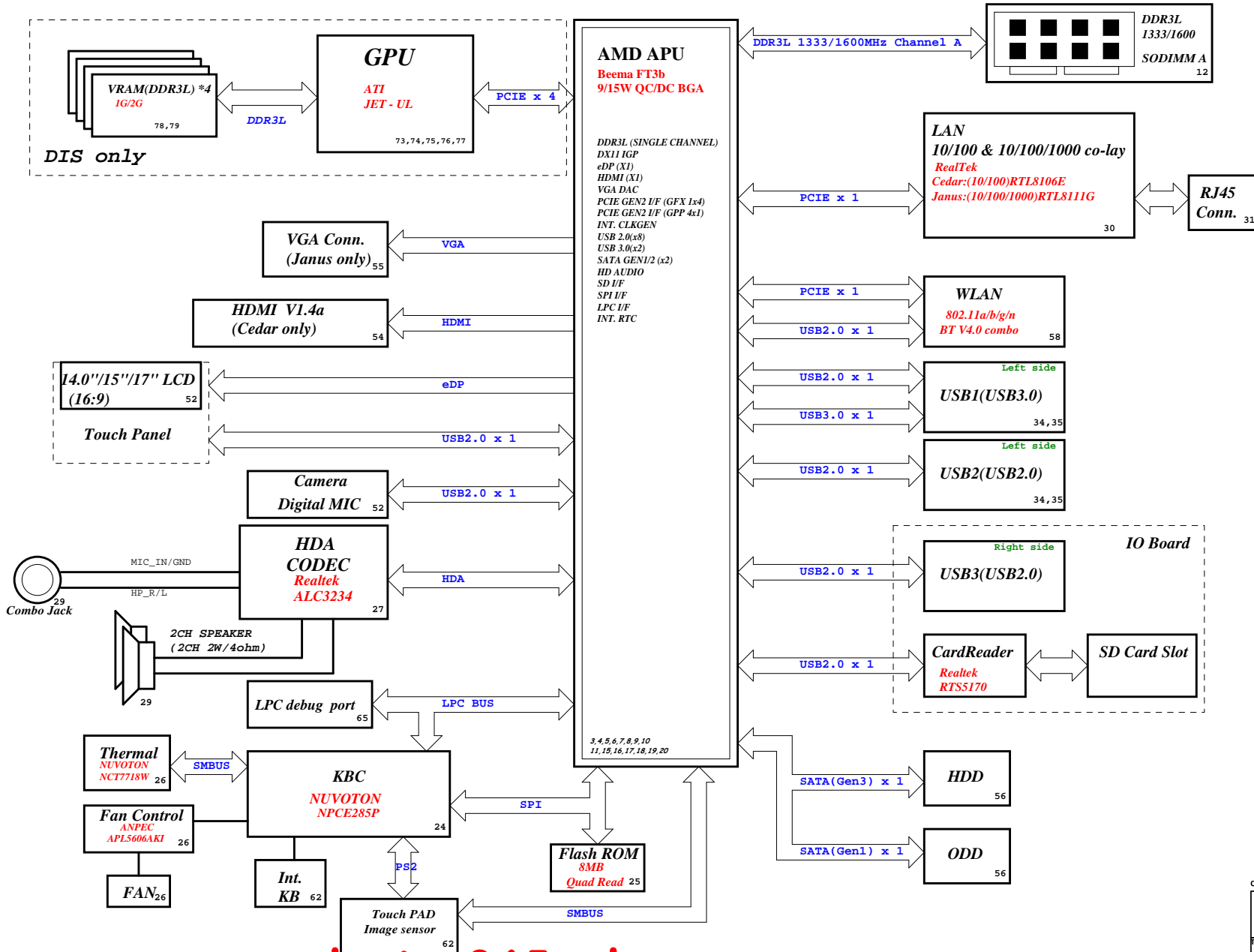
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Cedar UMA 14

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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Cover Page			
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Project code:4PD00G010001
PCB P/N: 13283-1
Revision: A00

Cedar Block Diagram



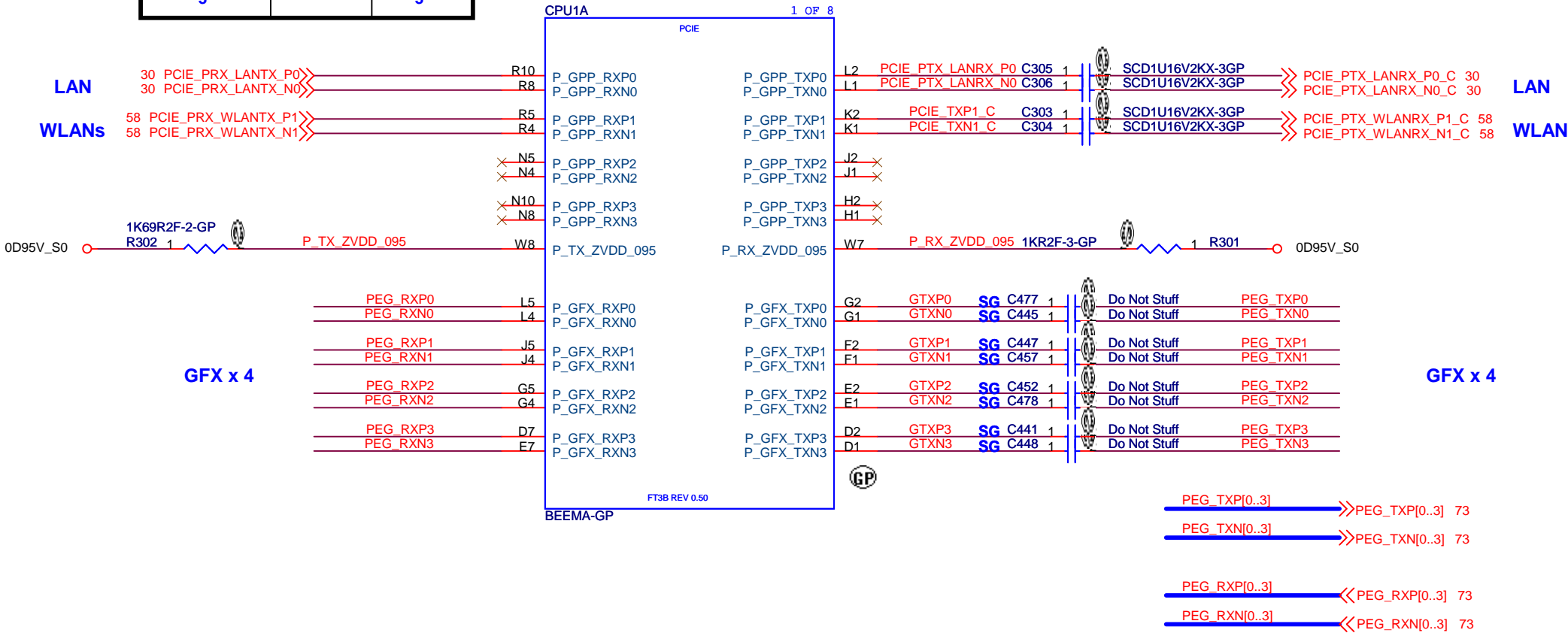
CHARGER	
BQ24727RGRR	44
INPUTS	OUTPUTS
AD+	DCBATOUT
BT+	
SYSTEM DC/DC	
TPS51225RUKR-GP	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5
CPU Core Power	
ISL95813HRZ-GP	46, 47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DDR3L SUS	
TPS51716RUKR-GP	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D65V_S0
CPU 1.05V	
RT8237CZQW-2-GP	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0
VDDIO_AZ	
TLV70215DBVR	36
INPUTS	OUTPUTS
3D3V_S5	1D5V_S0
Switches	
36	83
INPUTS	OUTPUTS
1D35V_S3	1D35V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0
0D95V_S5	0D95V_VGA_S0
3D3V_S0	3D3V_VGA_S0
1D35V_S3	1D35V_VGA_S0
1D8V_S5	1D8V_VGA_S0
PCB LAYER	
L1:TOP L2:VCC L3:Signal L4:Signal L5:GND L6:BOT	

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Block Diagram	
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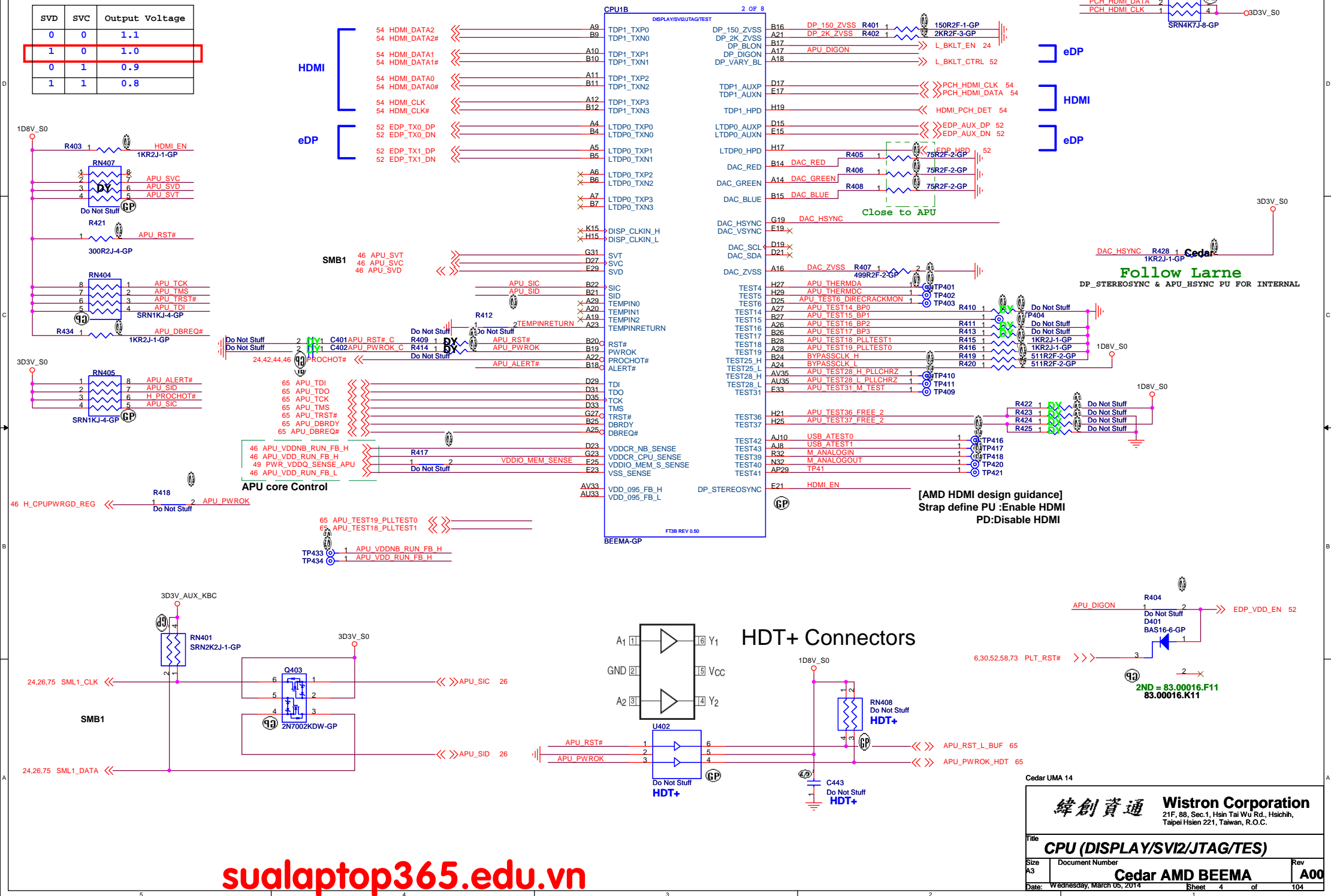
GPP CLK port	Device	CLKREQ#
0	LAN WLAN	0
1		1
2		2
3		3

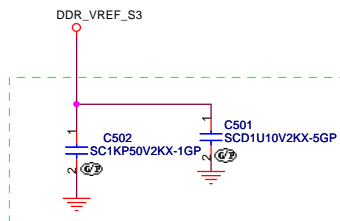
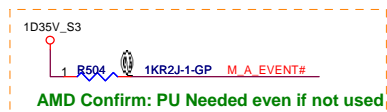


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Title		
CPU (PCIE)		
Size	Document Number	Rev
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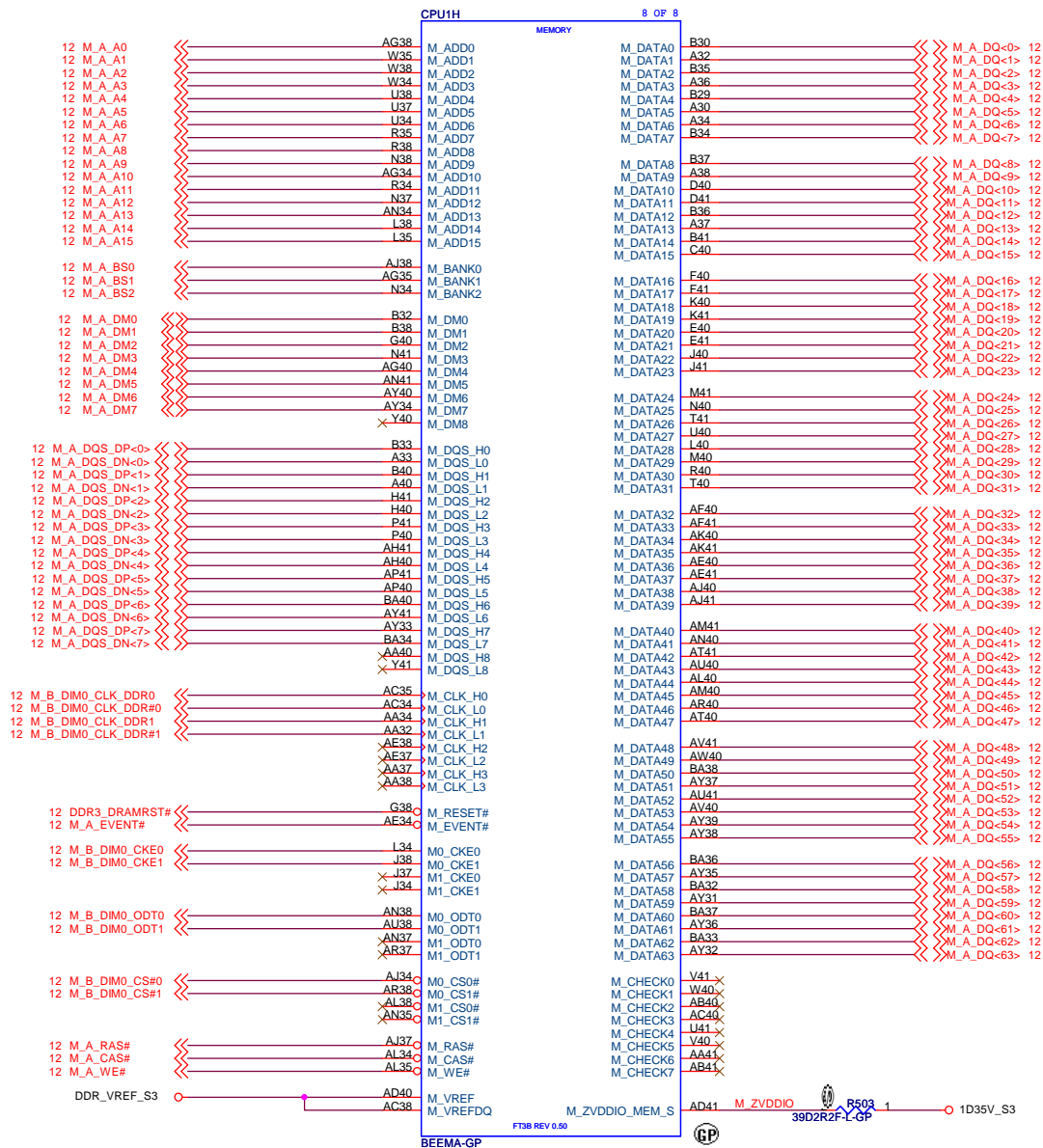
SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8





LAYOUT: place them close to APU

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There are integrated pull-up.

Pin	Function
R635	10KR2J-3-GP
R603	Do Not Stuff
R604	10KR2J-3-GP
R601	10KR2J-3-GP

Associated signals:

- BLUETOOTH_EN
- H_A20GATE
- KB_DET#
- DBC_EN

The diagram shows a horizontal timeline with two vertical dashed lines. The first dashed line is labeled '24.65 LPC_RST# <<' on the left. The second dashed line is labeled 'LPC_RST#_C' on the right. Between these two lines, there is a blue horizontal bar labeled 'R602' above it and 'Do Not Stuff' below it. The bar is flanked by the numbers '1' and '2' at its ends.

CEDAR_JANUS_ID	
1	CEDAR
0	JANUS

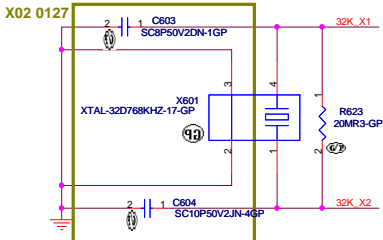
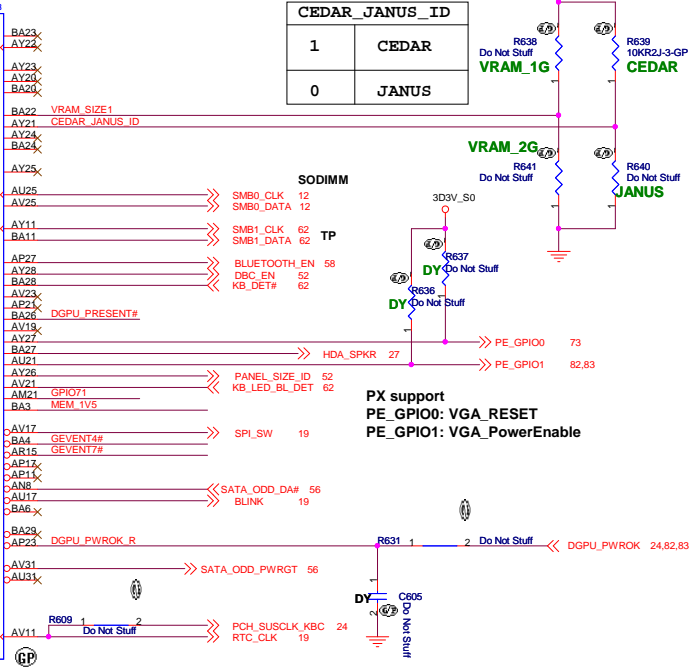
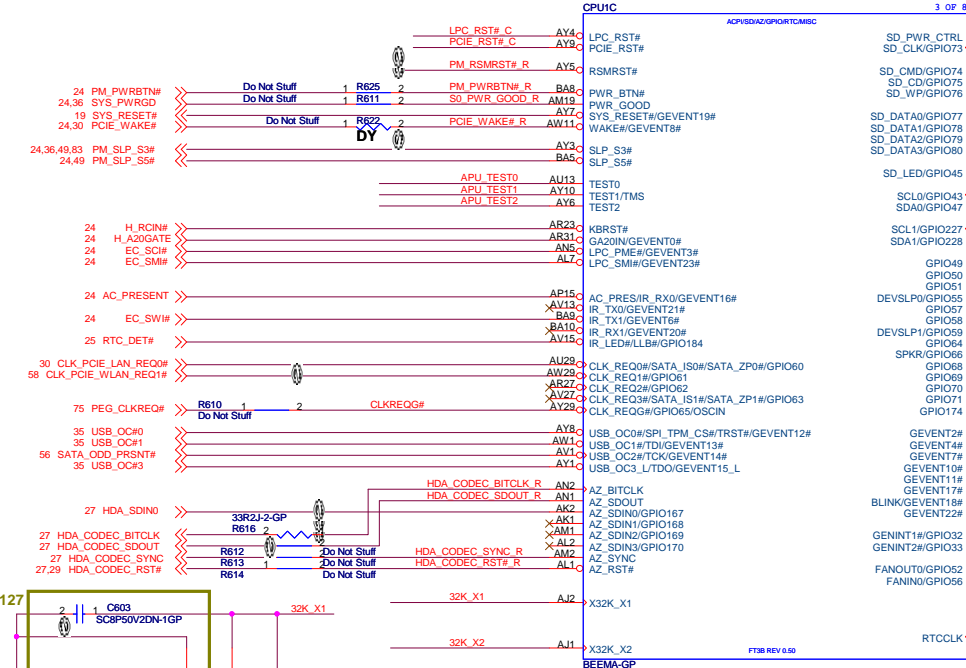
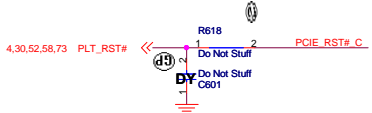
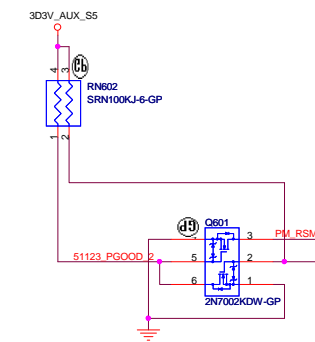
KBC need to use OD Type

1D8V_S5

R627

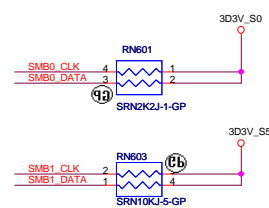
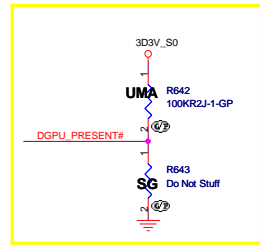
10KR2J-3-GP

S0 PWR GOOD R

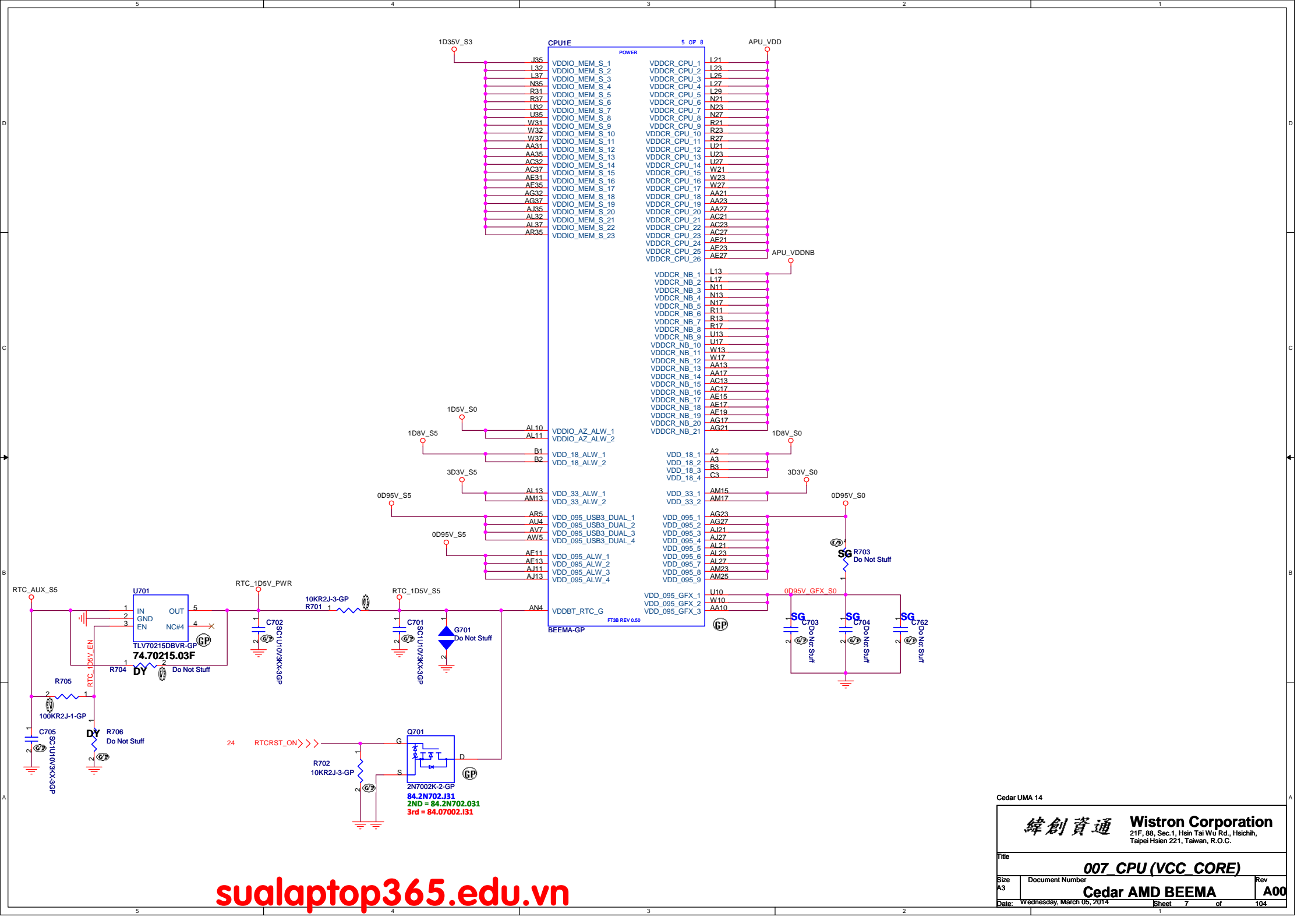


	XTAL	CLK, Hz
0	System & USB	48M
1	RTC	32.768K
2	LAN	25M
3	VGA	27M

AMD suggests Xtal ESR must be less than 65R

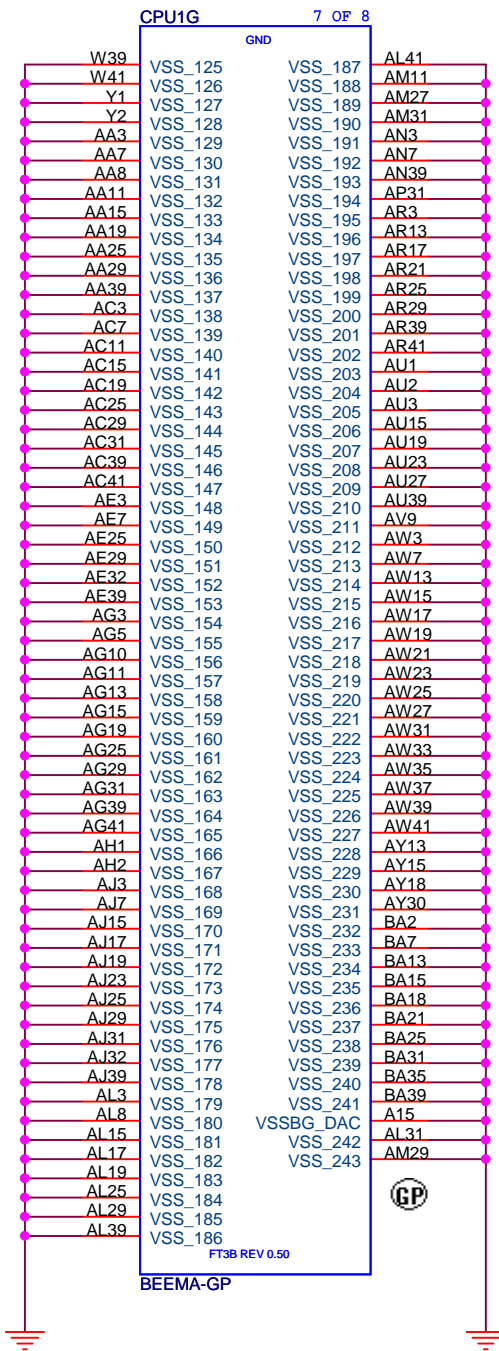
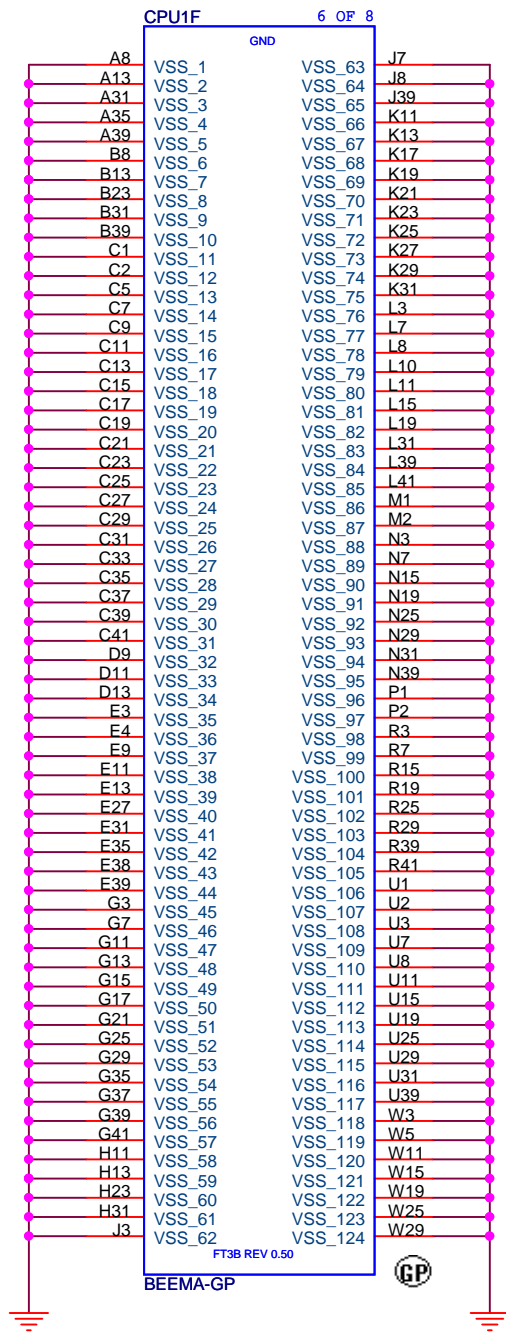
Report APU
H=UMA L=DISCRETE

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Title

CPU (VSS)

Size
A4

Document Number

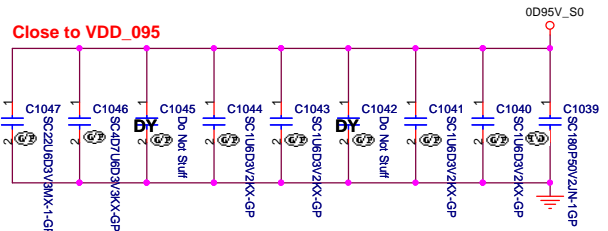
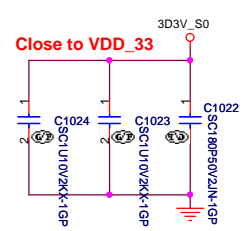
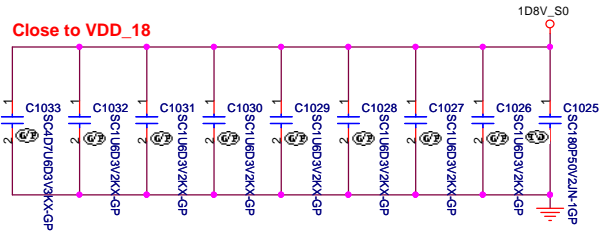
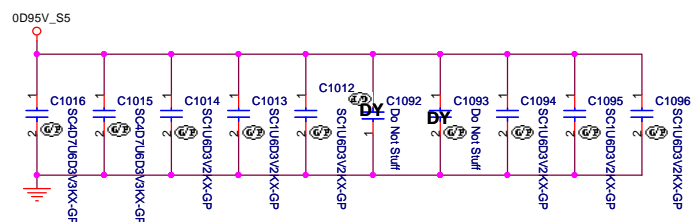
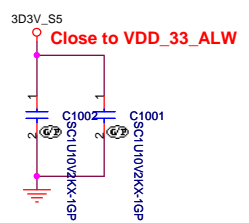
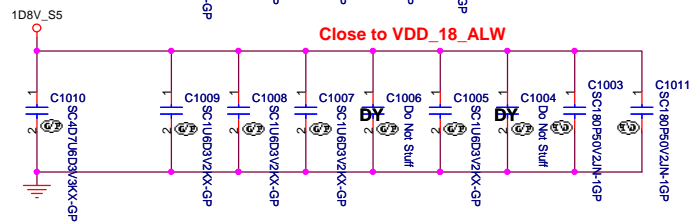
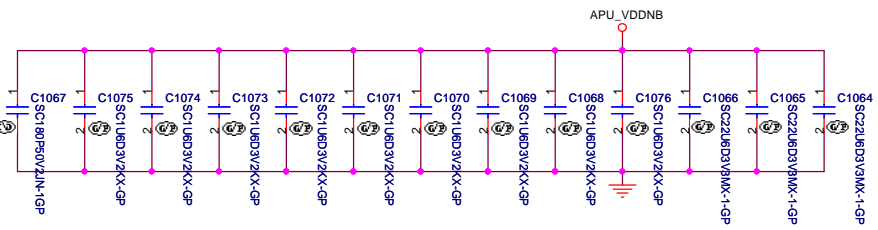
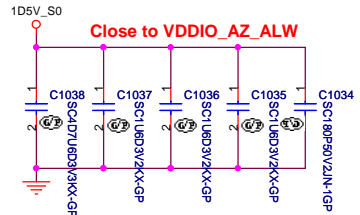
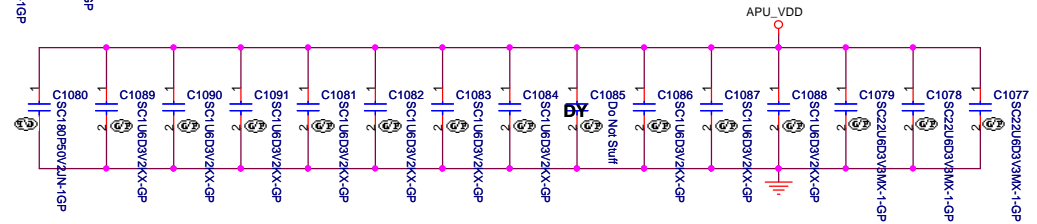
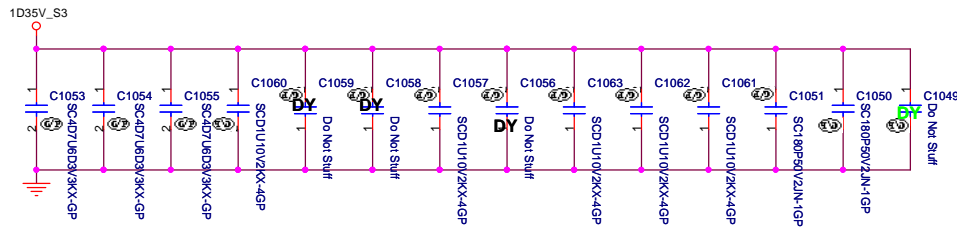
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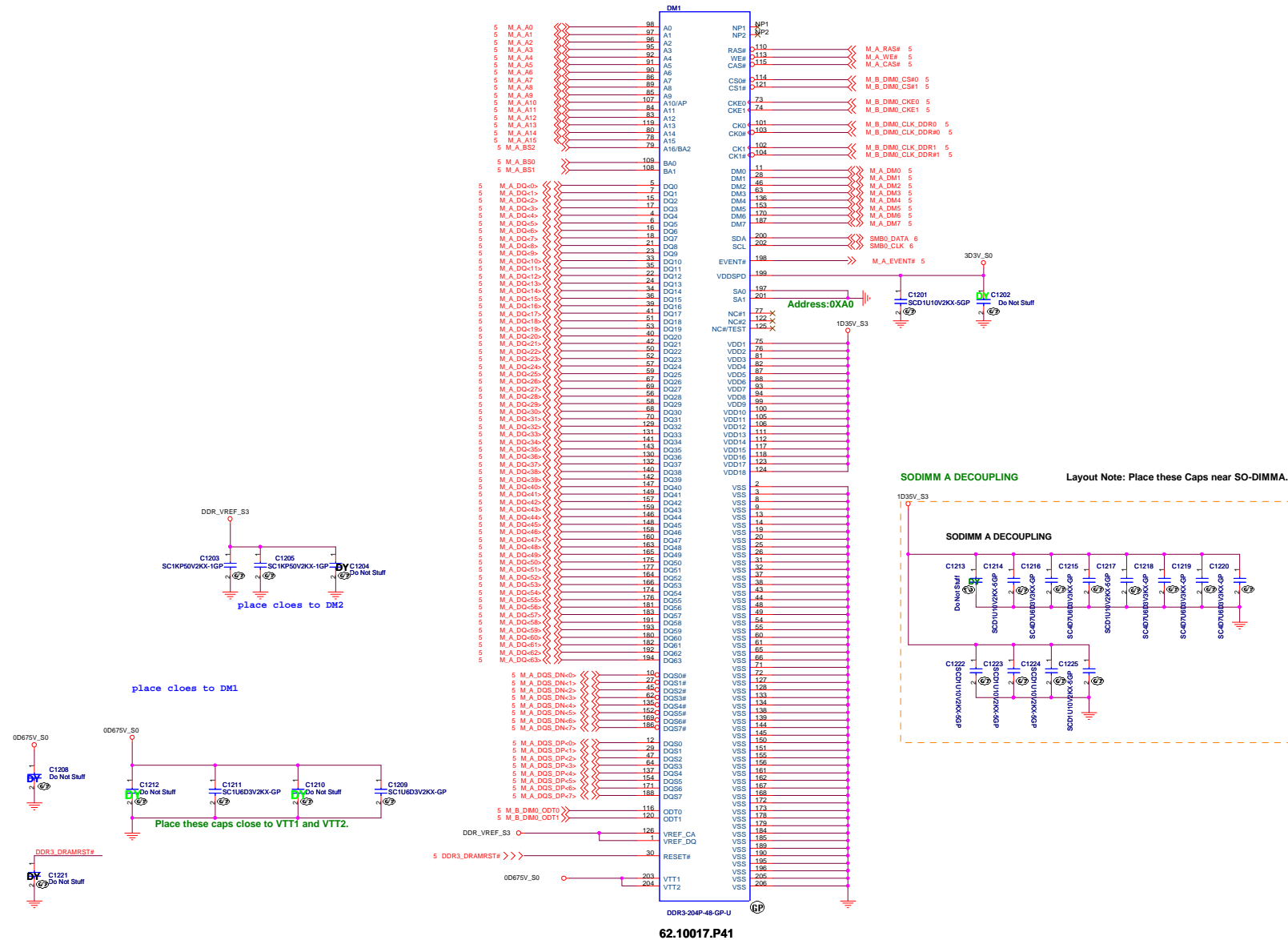


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SSID = MEMORY



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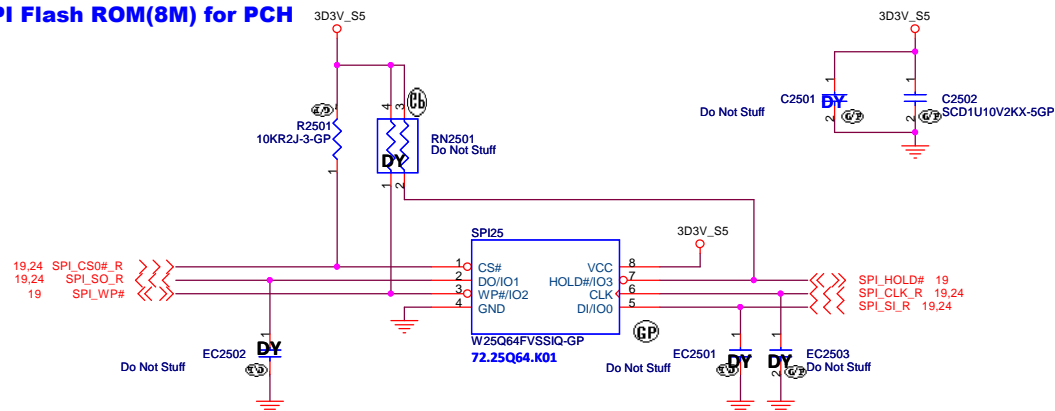
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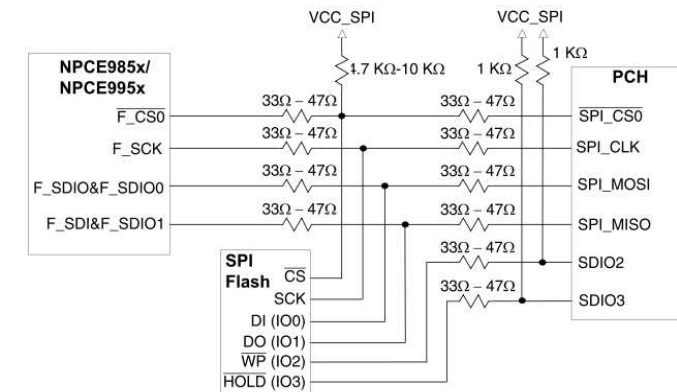
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



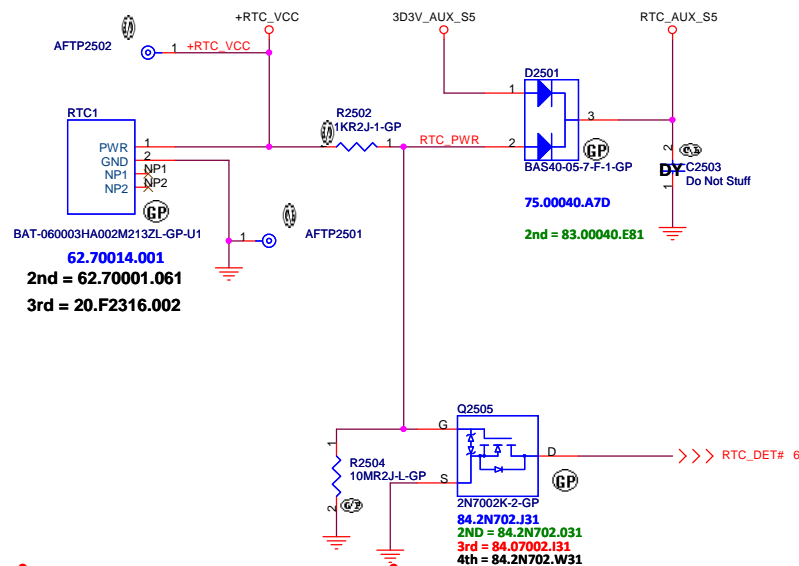
Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	o	o
72.25647.00A	o	o

Single SPI shared flash connection (SPI Quad I/O mode)



Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT



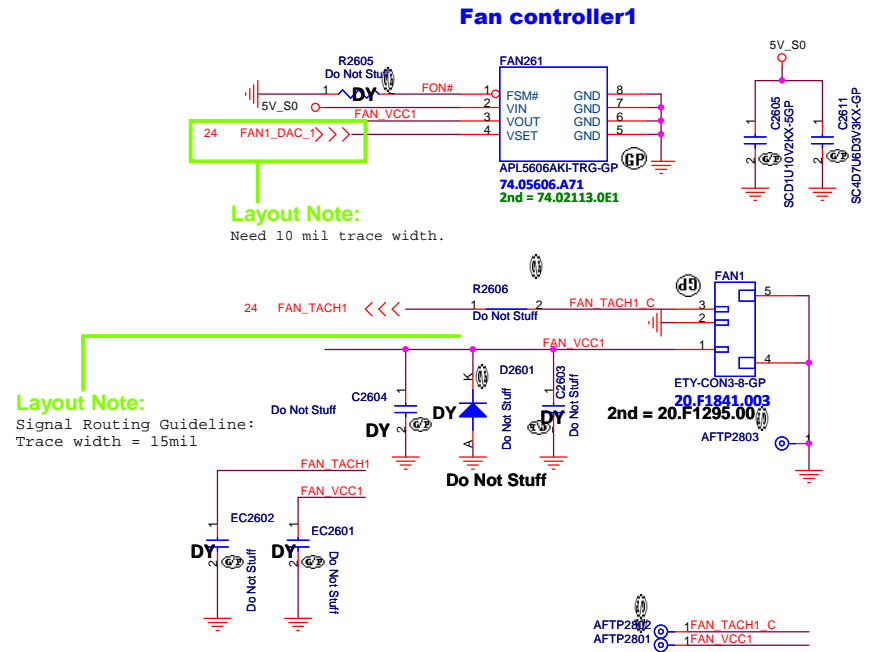
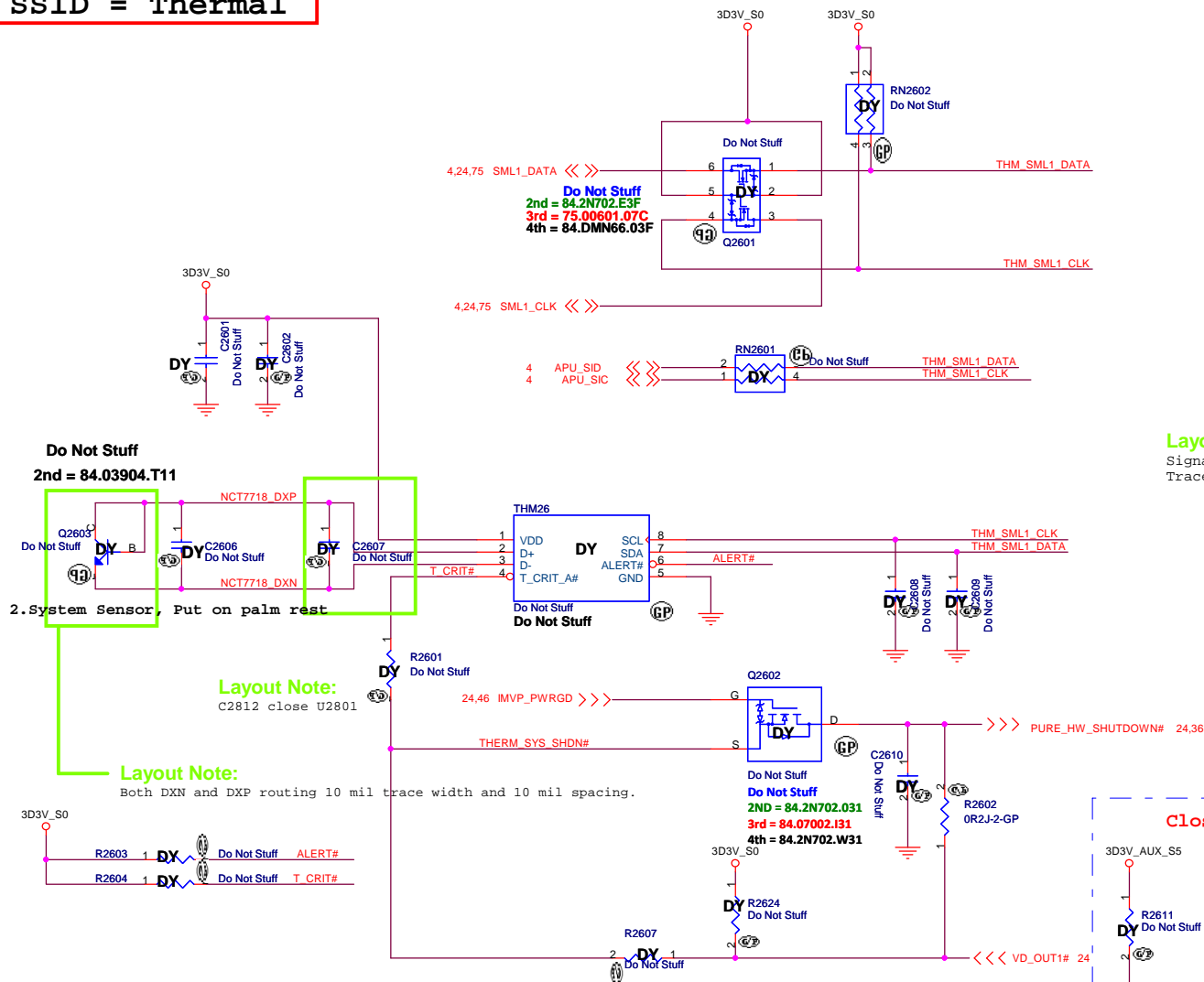
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Flash/RTC		
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SSID = Thermal



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

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Title

THERMAL NCT7718W/Fan

Size

Document Number	
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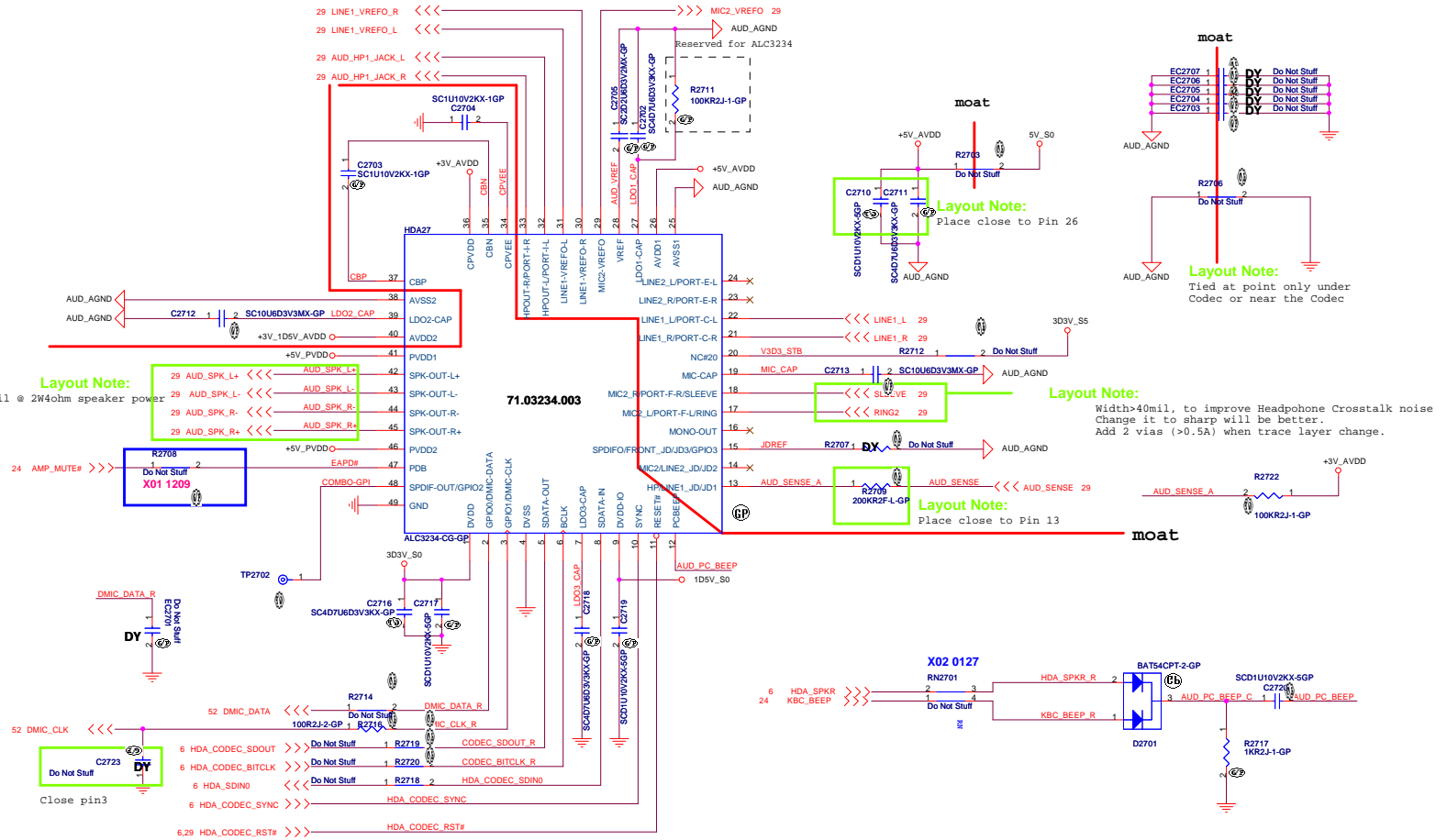
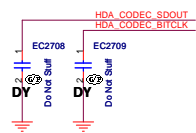
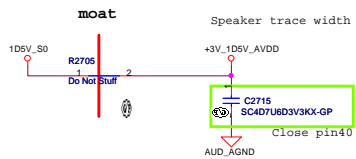
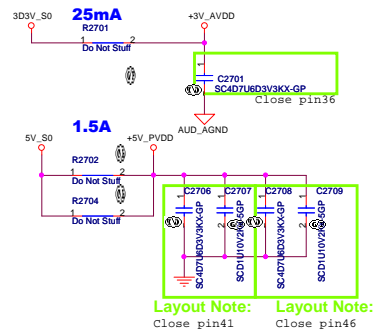
Date _____

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SSID = AUDIO



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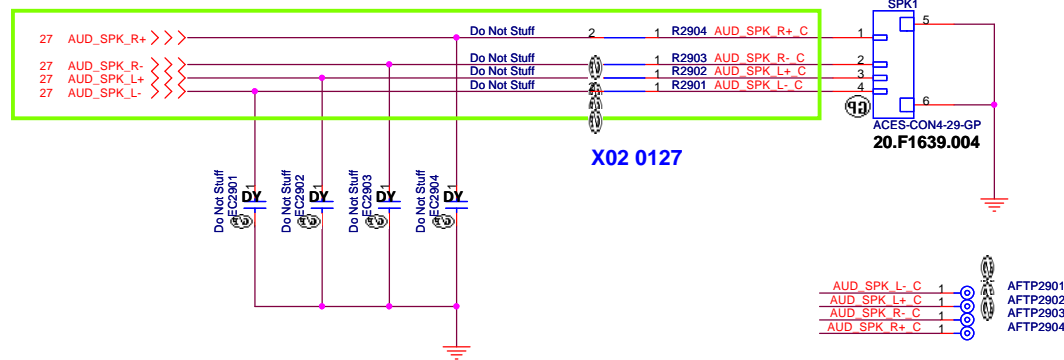
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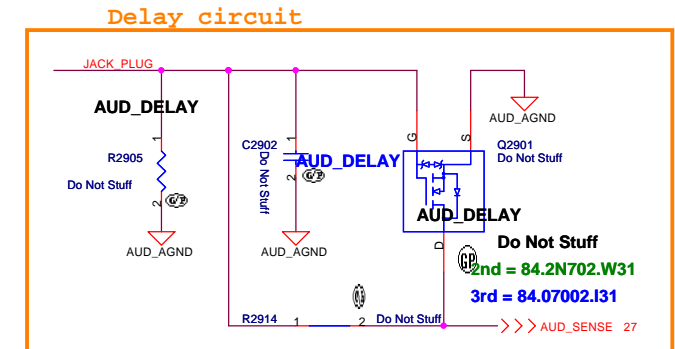
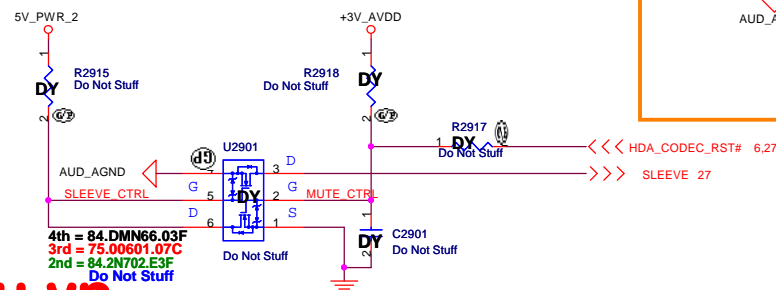
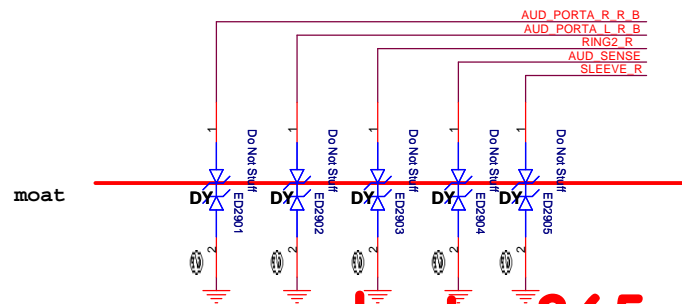
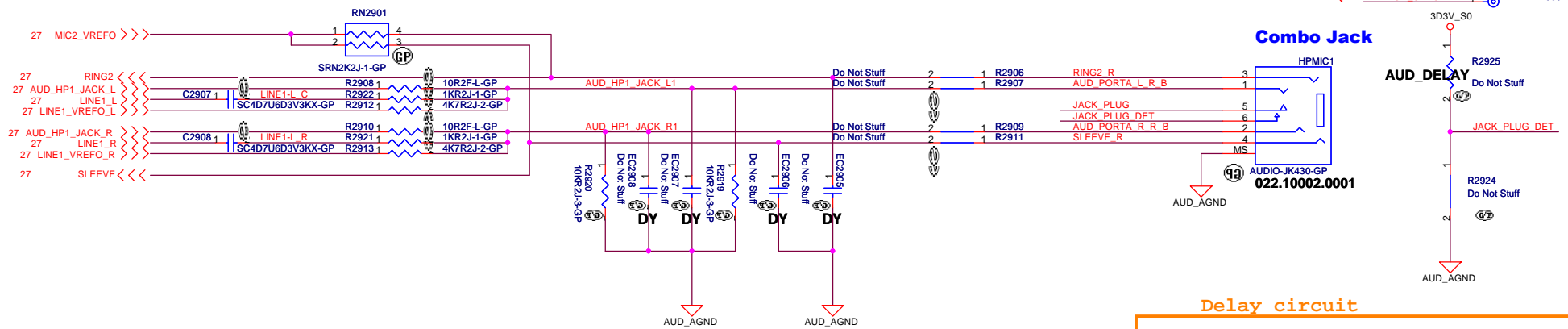
SSID = AUDIO

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



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Title
Thermal NCT7718W/Fan Controllor P2793

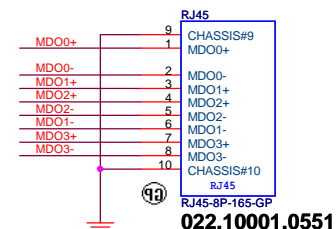
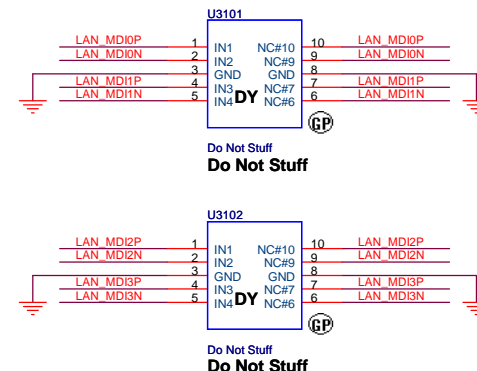
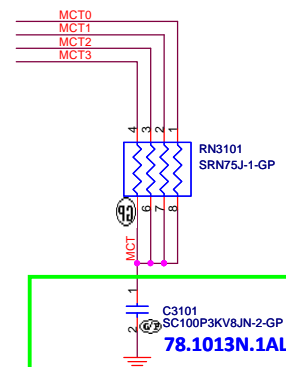
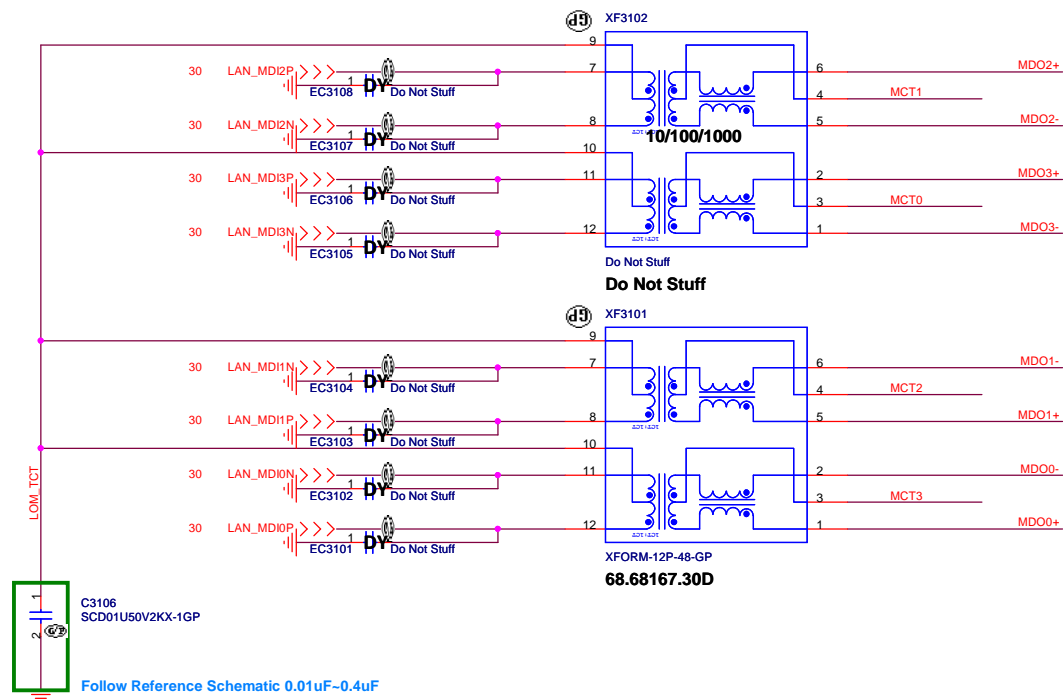
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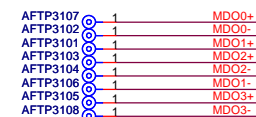
SSID = LOM

LAN TransFormer (10/100/1000M & 10/100M co-lay)

Layout note:
30 mil spacing between MDI differential pairs.



Layout:
Place near RJ45



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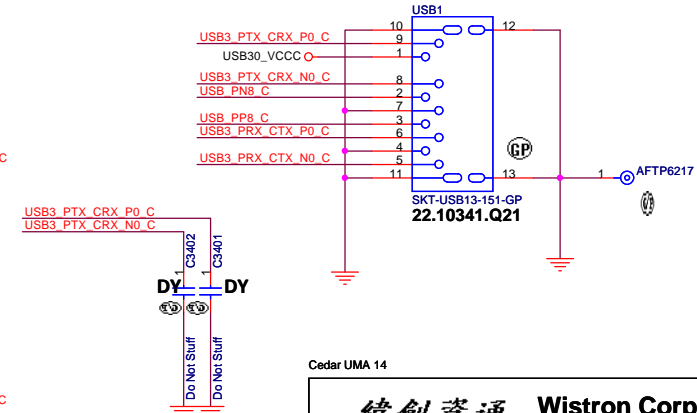
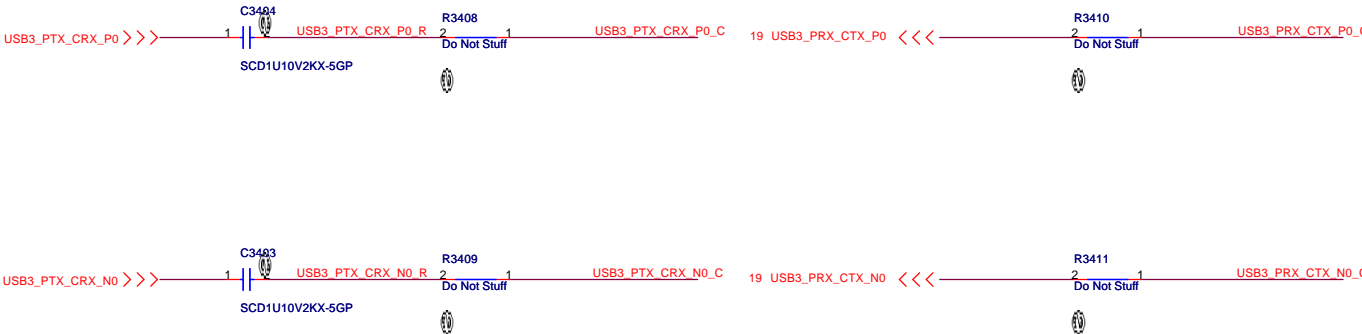
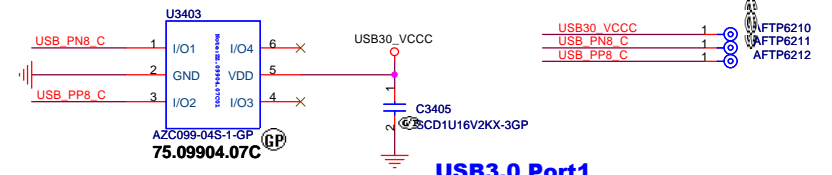
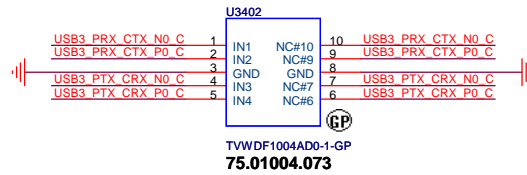
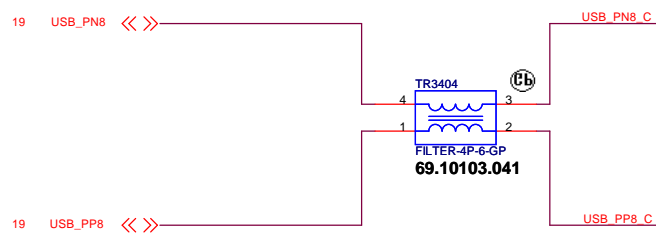
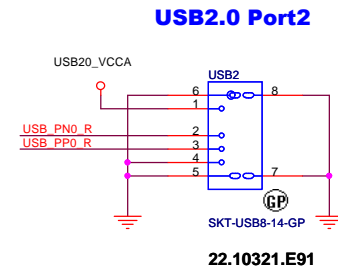
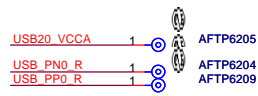
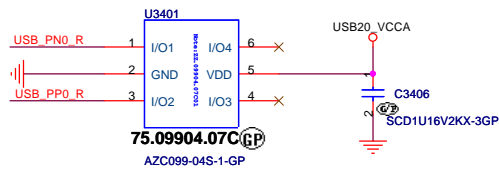
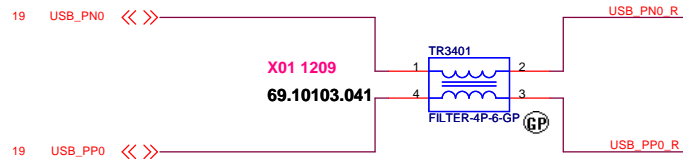
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)Card Reader			
Size A4	Document Number Cedar AMD BEEMA		Rev A00
Date:	Wednesday, March 05, 2014	Sheet 32 of	104

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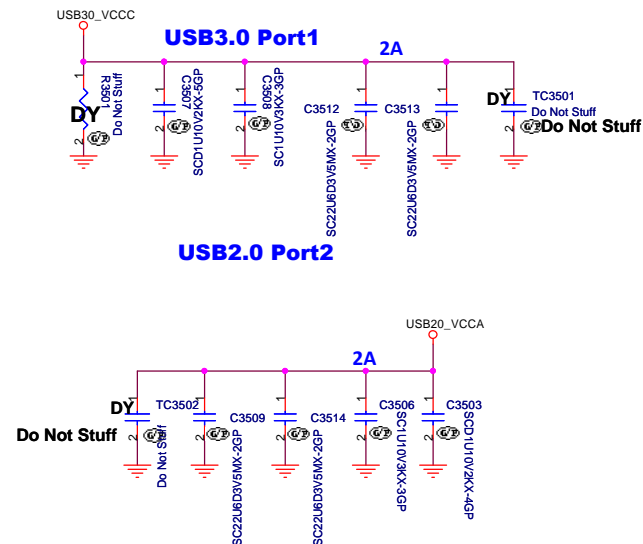
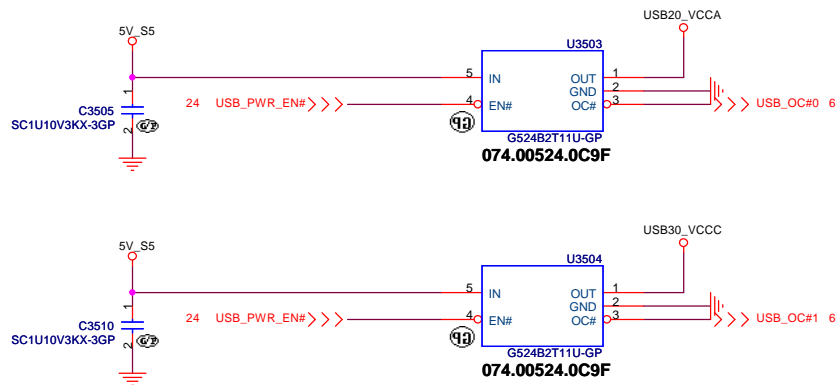
Cedar UMA 14

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size A4	Document Number Cedar AMD BEEMA		Rev A00
Date:	Wednesday, March 05, 2014	Sheet 33 of	104

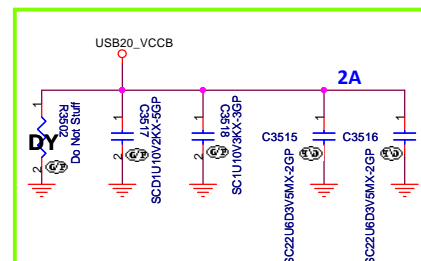
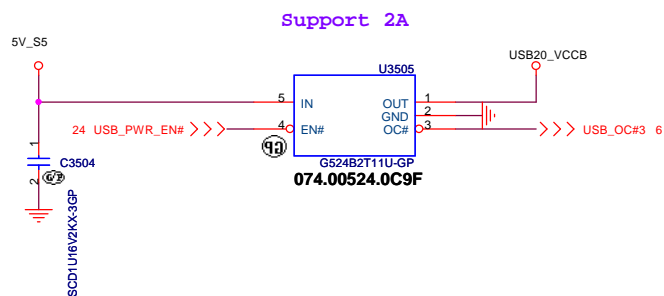
SSID = USB



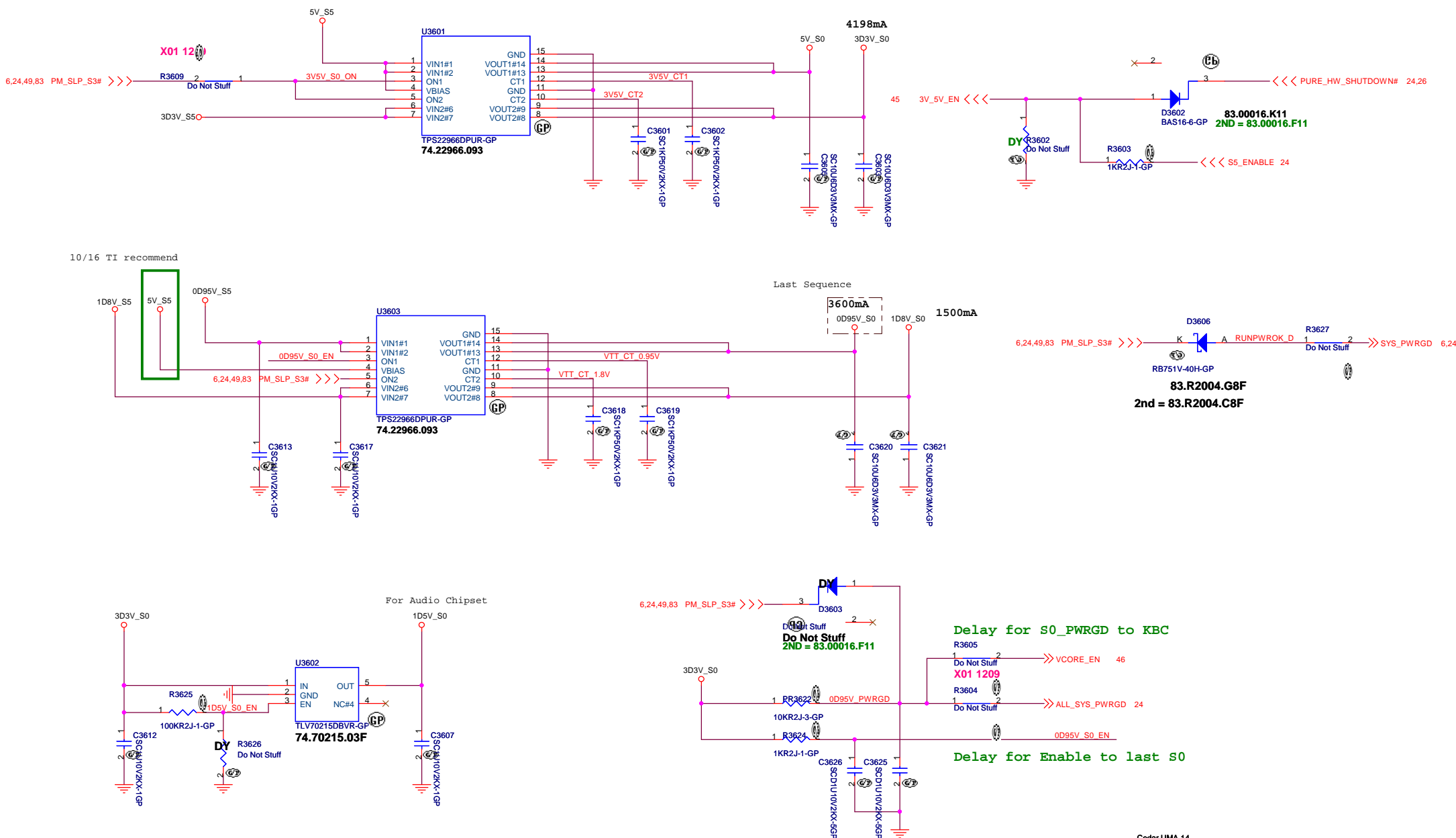
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Layout Note: Close CON1



Power Sequence



Cedar UMA 14

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
Power Plane Enable			
Size A3	Document Number		Rev
	Cedar AMD BEEMA		A00
Date:	Wednesday, March 05, 2014	Sheet 36 of	104

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SSID = Reset.Suspend

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<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div> <div>(Reserved)</div>			
<div>Size</div> <div>A4</div>	<div>Document Number</div> <div>Cedar AMD BEEMA</div>		<div>Rev</div> <div>A00</div>
<div>Date</div> <div>Wednesday, March 05, 2014</div>		<div>Sheet</div> <div>38</div>	<div>of</div> <div>104</div>


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Cedar UMA 14

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>(Reserved) 1D05_M</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
Date: Wednesday, March 05, 2014		Sheet 39 of 104

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Cedar UMA 14

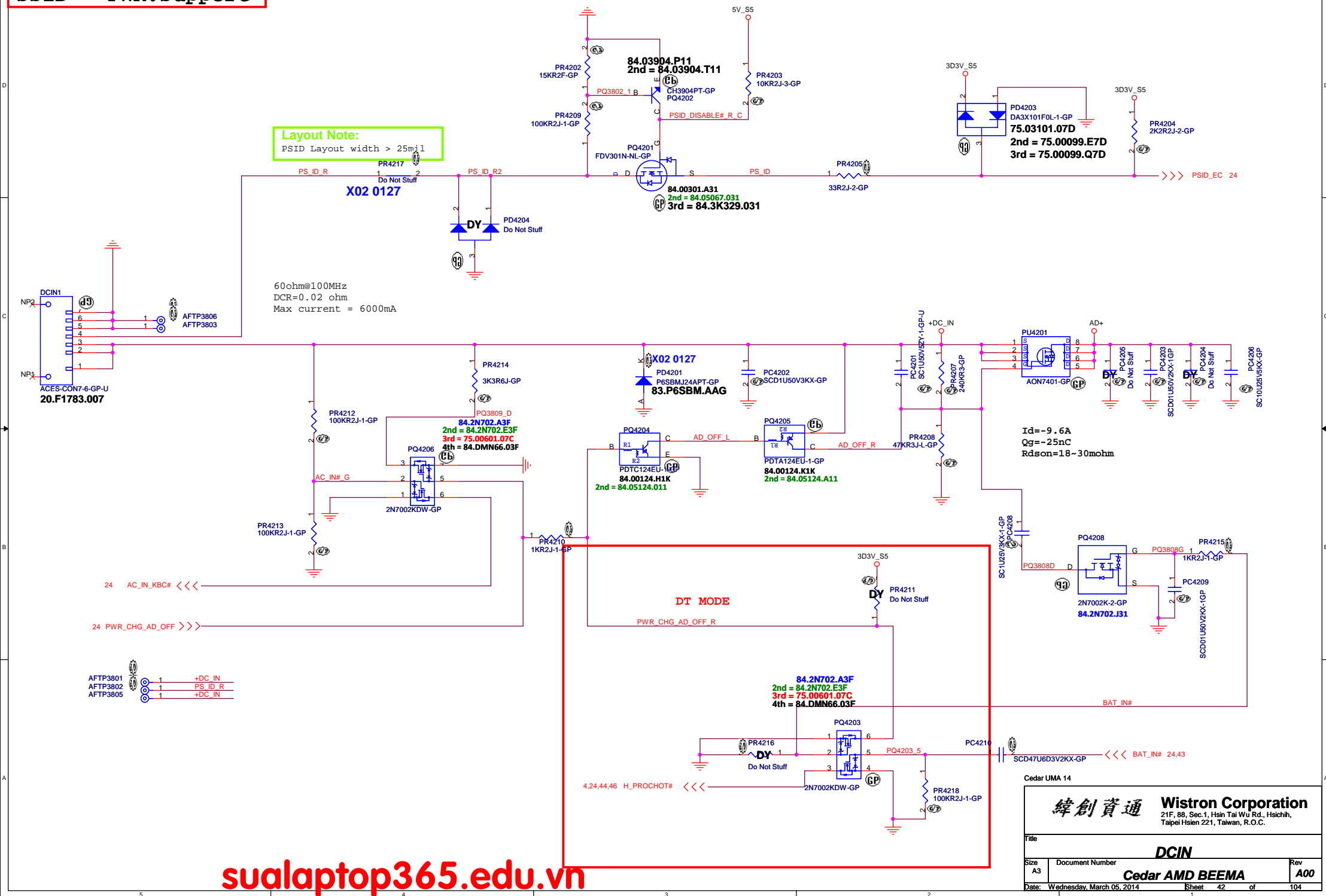
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Reserved		
Size A4	Document Number Cedar AMD BEEMA	Rev A00
Date: Wednesday, March 05, 2014		Sheet 40 of 104

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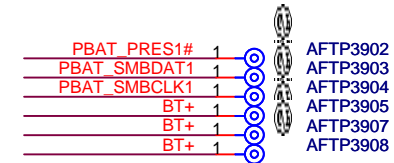
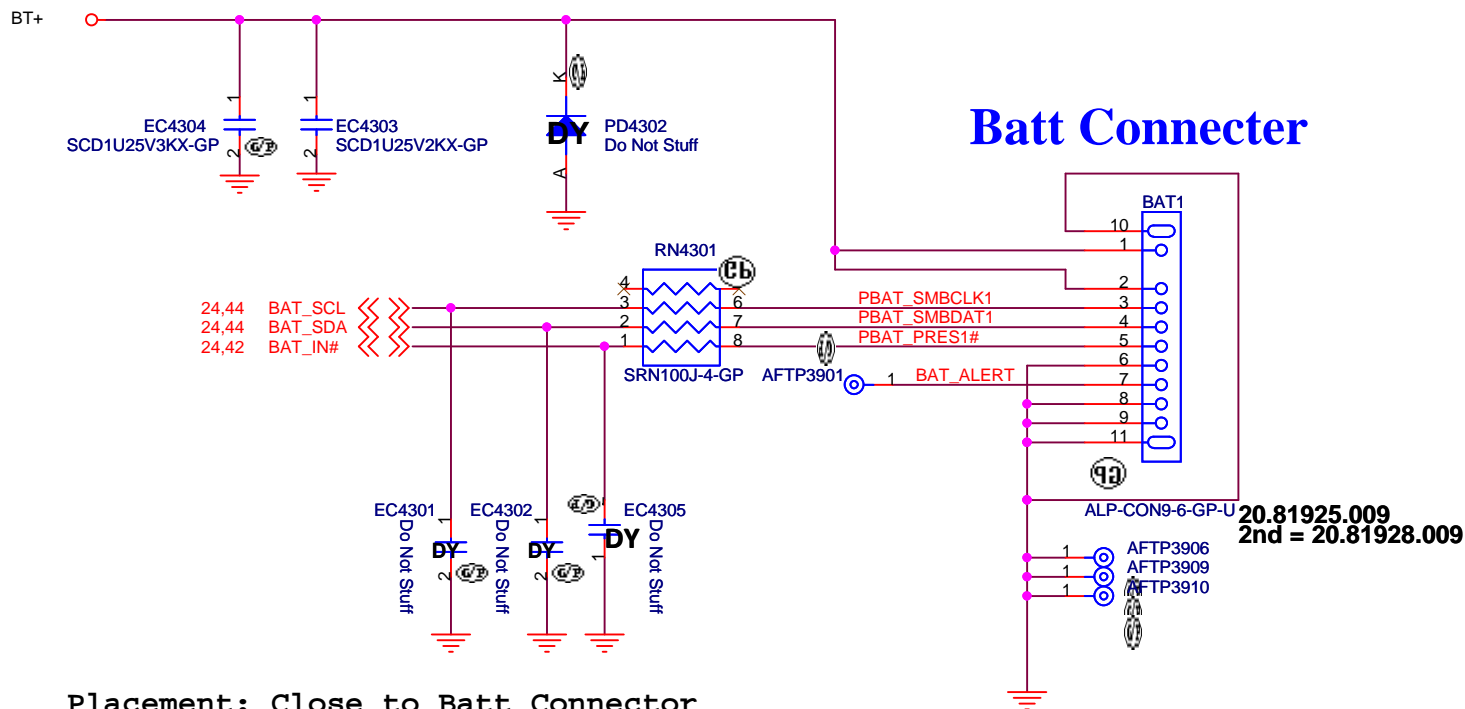
Cedar UMA 14

<div>緯創資通</div>		<div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
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Size A4	Document Number <div>Cedar AMD BEEMA</div>		Rev A00
Date: Wednesday, March 05, 2014	Sheet 41	of	104

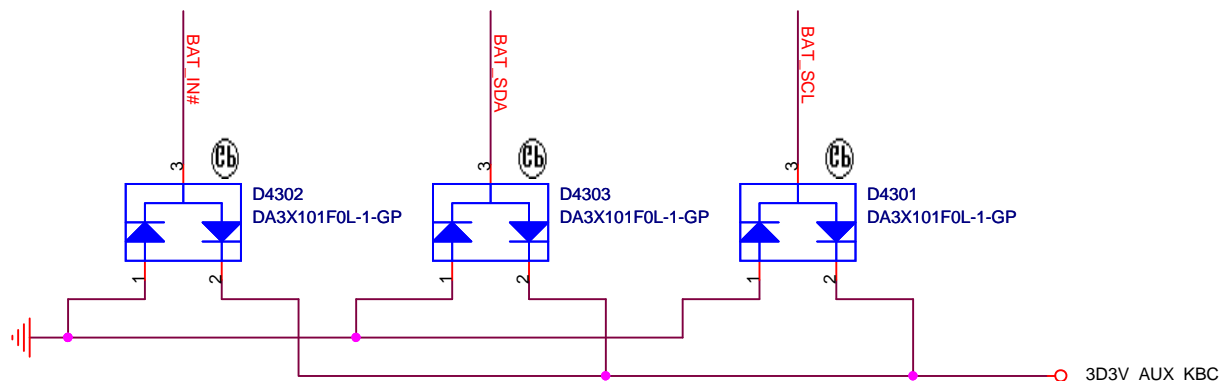
SSID = PWR.Support



SSID = PWR.Support



Placement: Close to Batt Connector



75.03101.07D

75.03101.07D

75.03101.07D

2nd = 75.00099.E7D

2nd = 75.00099.E7D

2nd = 75.00099.E7D

3rd = 75.00099.Q7D

3rd = 75.00099.Q7D

3rd = 75.00099.Q7D

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緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BATT CONN

Size
A4

Document Number

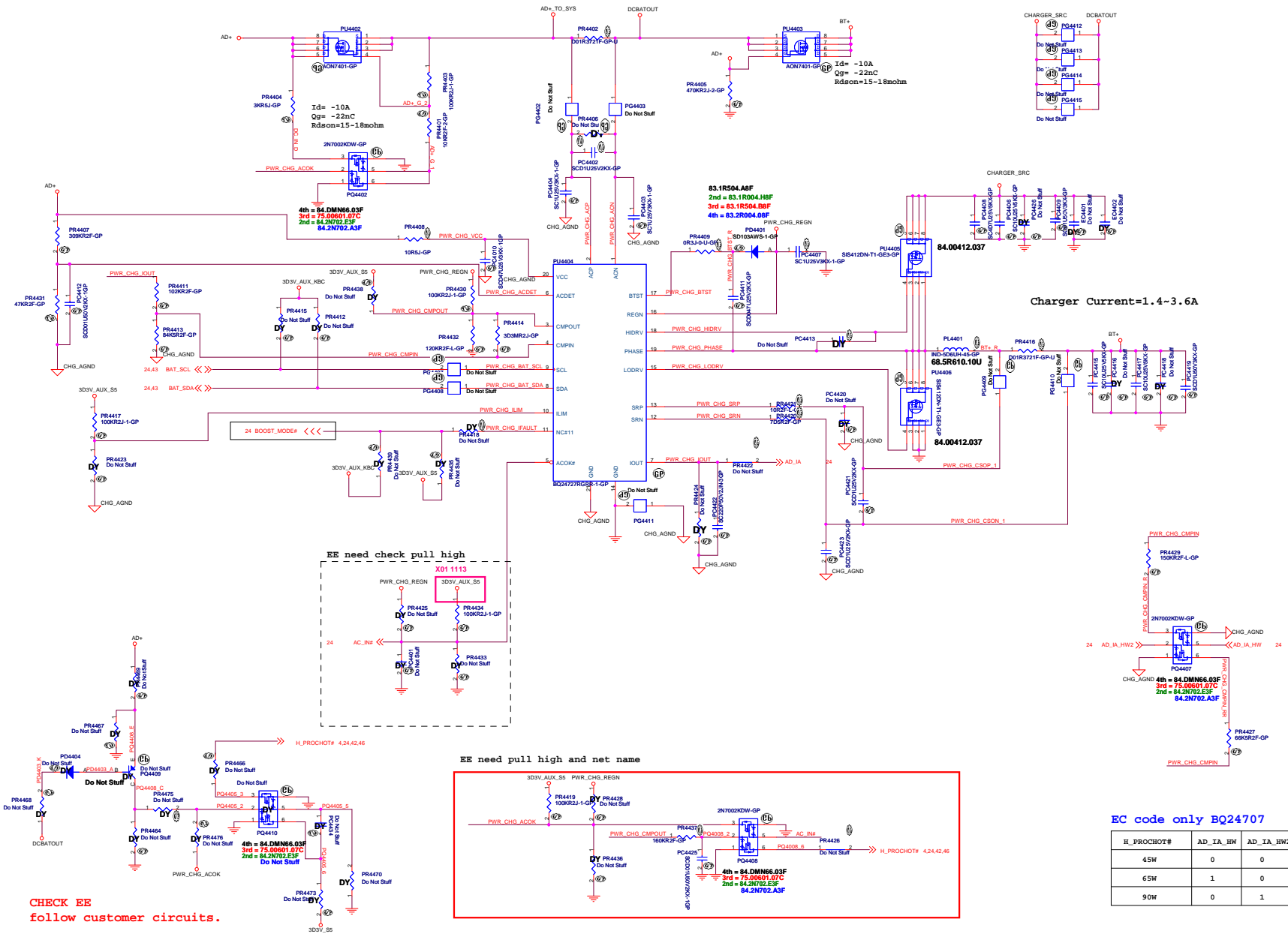
Cedar AMD BEEMA

Rev
A00

Date: Wednesday, March 05, 2014

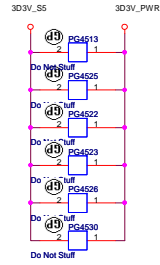
Sheet 43 of 104

SSID = Charger

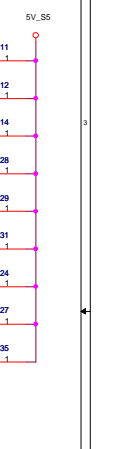
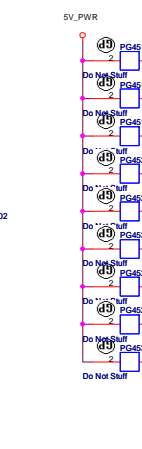
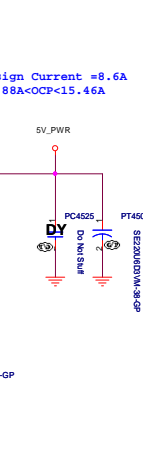
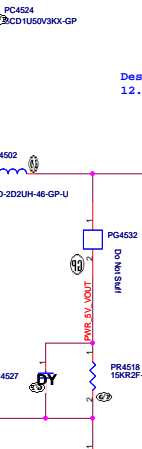
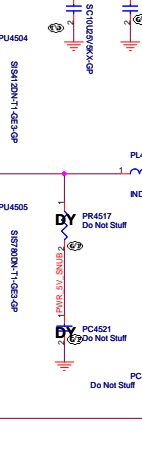
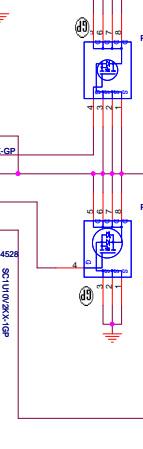
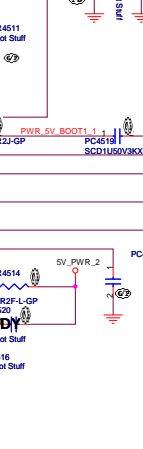
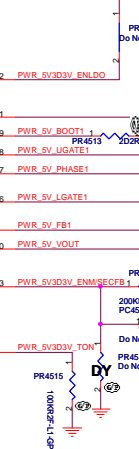
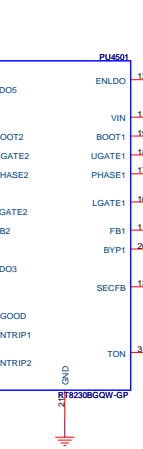
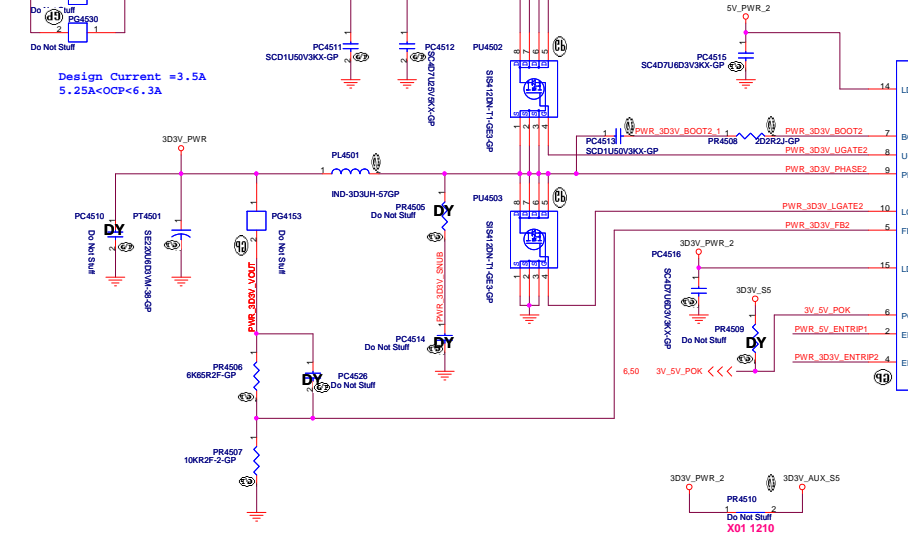
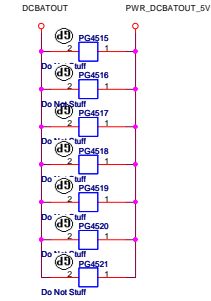
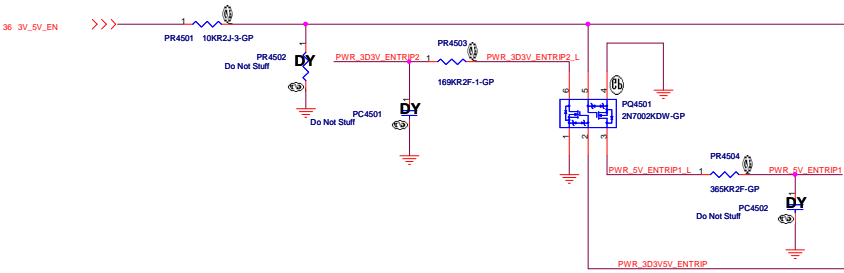
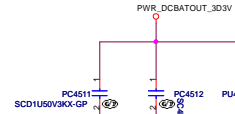
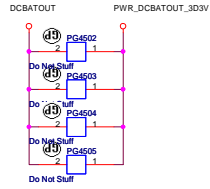


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SSID = PWR.Plane.Regulator_5v3p3v



Design Current =3.5A
5.25A<OCP<6.3A

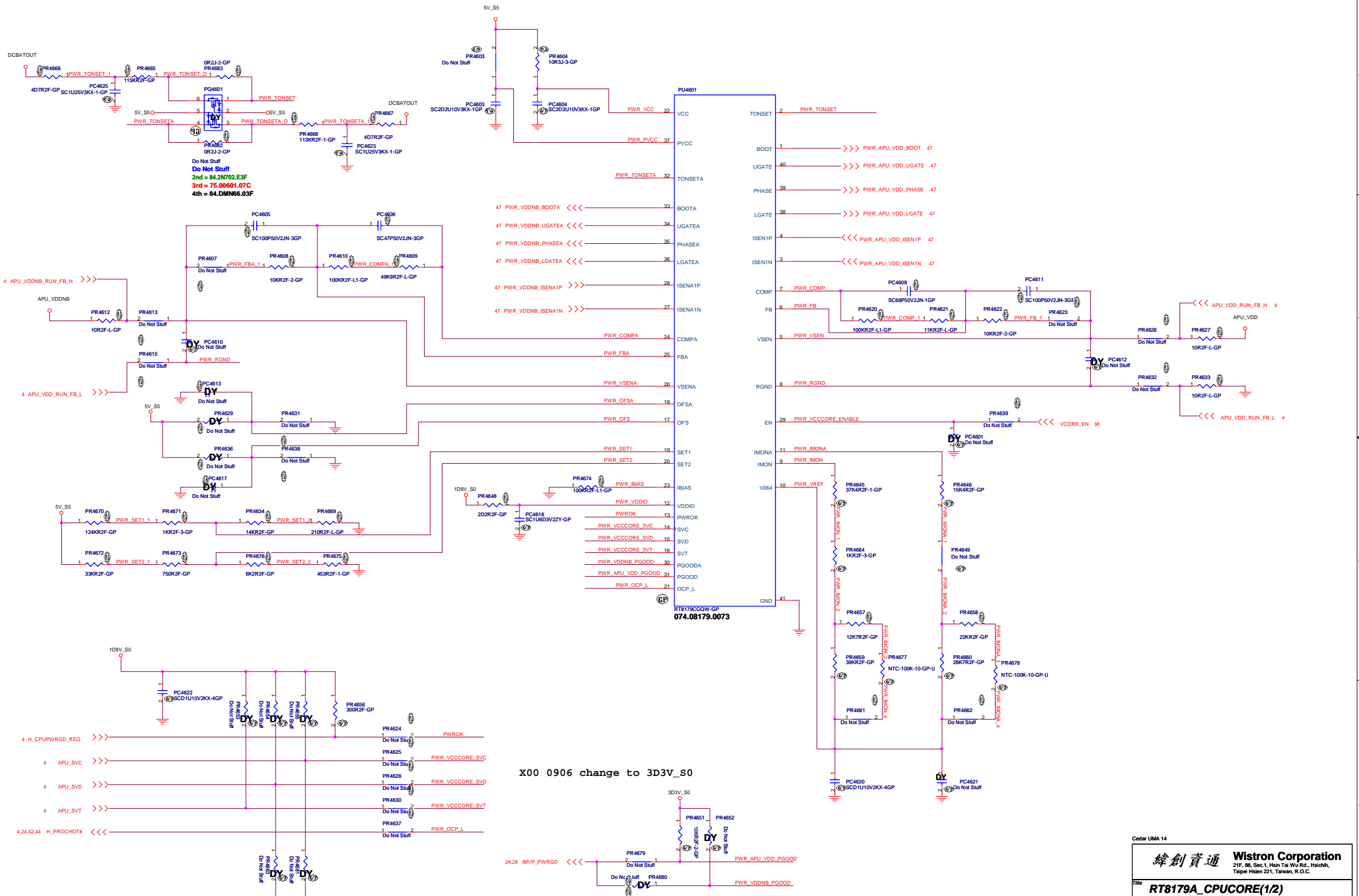


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R210.20A
O/P cap:CHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

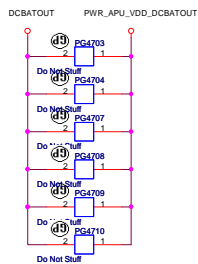
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Inductor: CHIP CHOK 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

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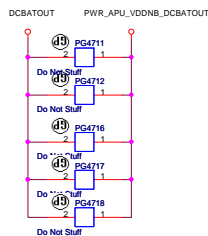
SSID = CPU.Regulator



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46 PWR_APU_VDD_UGATE >>>
 46 PWR_APU_VDD_LGATE >>>
 46 PWR_APU_VDD_PHASE >>>
 46 PWR_APU_VDD_BOOT >>>
 46 PWR_APU_VDD_SEN1P <<<
 46 PWR_APU_VDD_SEN1N <<<



46 PWR_VDDNB_UGATE >>>
 46 PWR_VDDNB_LGATE >>>
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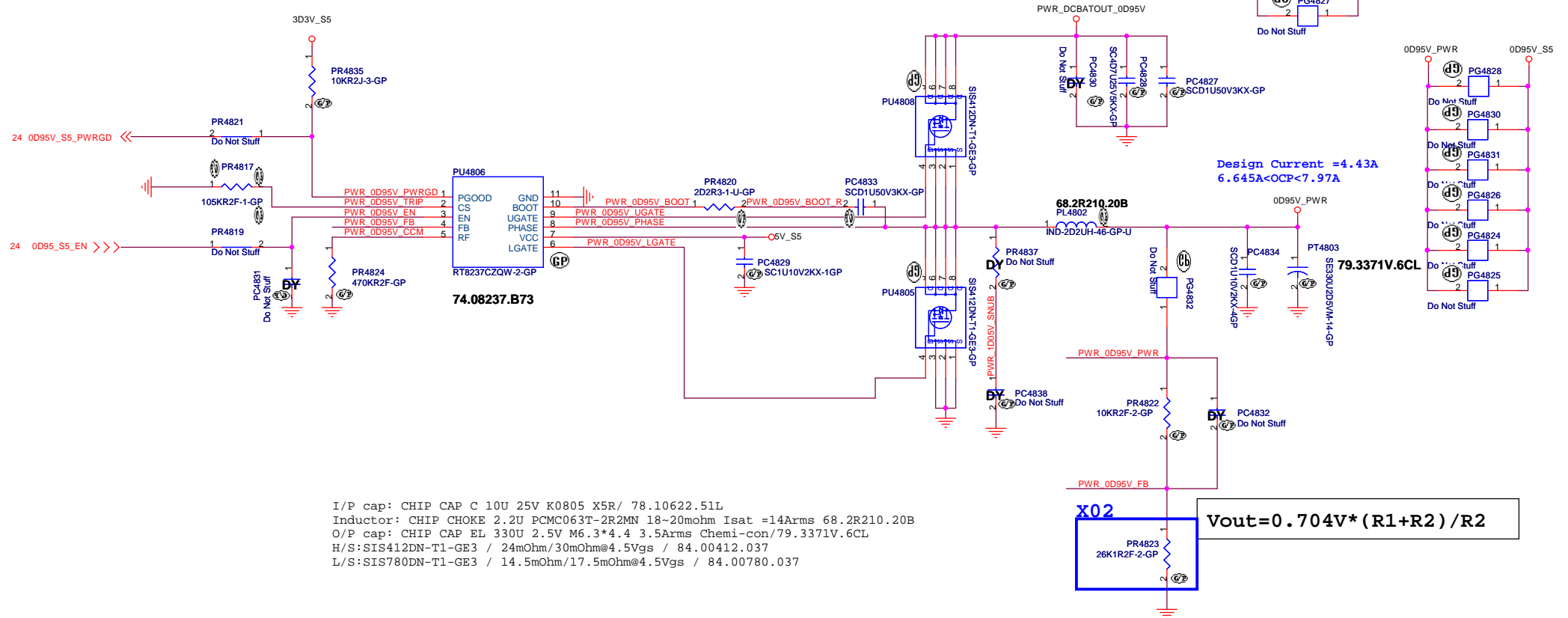
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 Inductor: CHIP CHOK 0.36UH PCMR0647T-R36MS1R407 1.4mohm / Isat =24Arms 68.R3610.20W
 O/P cap:CHIP CAP 470UF 2V EEFSX0D471X /Panasonic/ 6mohm / 79.47719.2BL
 Dual N FET MOS SI2920DT-T1-GE3 DUAL NC POWER 8P /H/S 7.4mohm/8.9mohm / L/S 2.9mohm/3.5mohm@4.5Vgs / 84.00920.037

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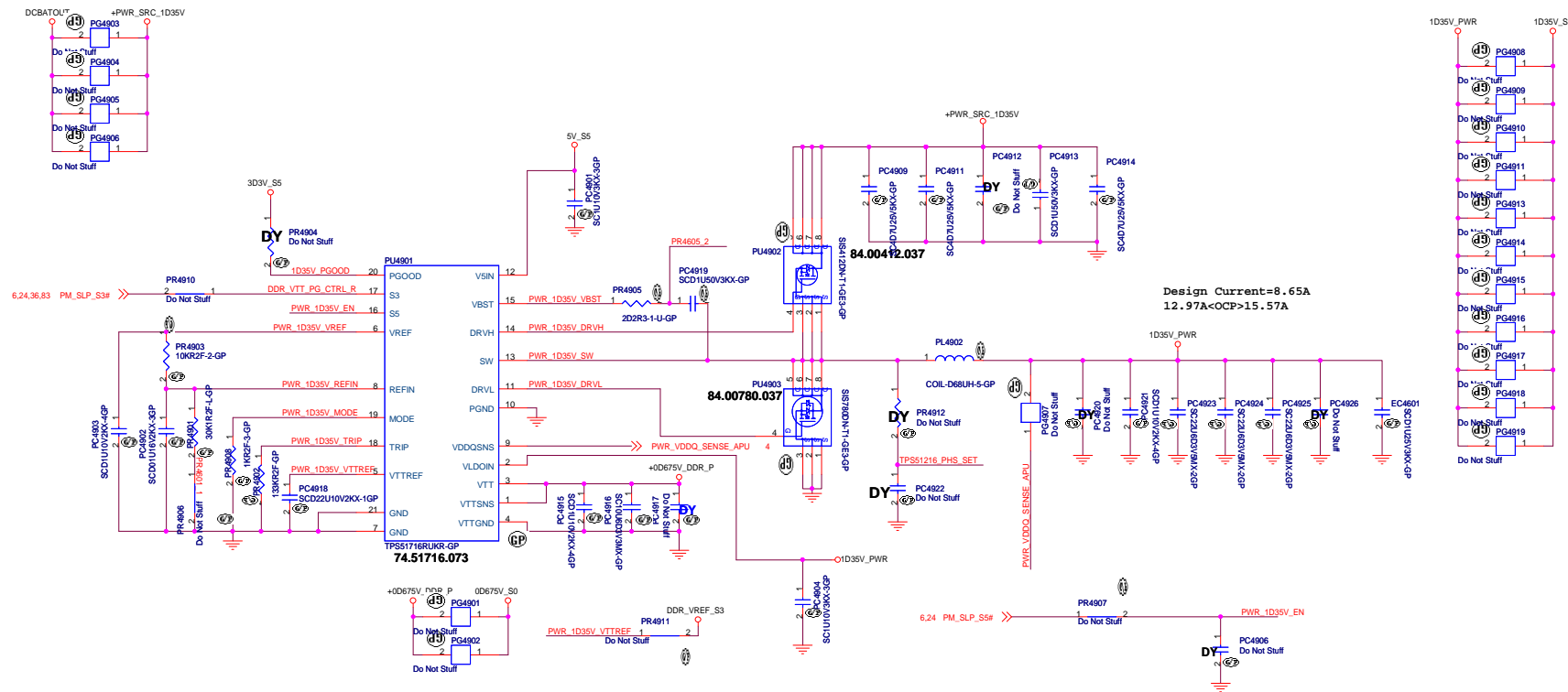
緯創資通 Wistron Corporation	
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.	
File	RT8179A_CPUCORE(22)
Size	A2
Document Number	Cedar AMD BEEMA
Date	Wednesday, March 06, 2014
Sheet	47 of 104
Rev	A00

SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
O/P cap: CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/79.3371V.6CL
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037


```
SSID = PWR.Plane.Regulator 1p35v0p675v
```



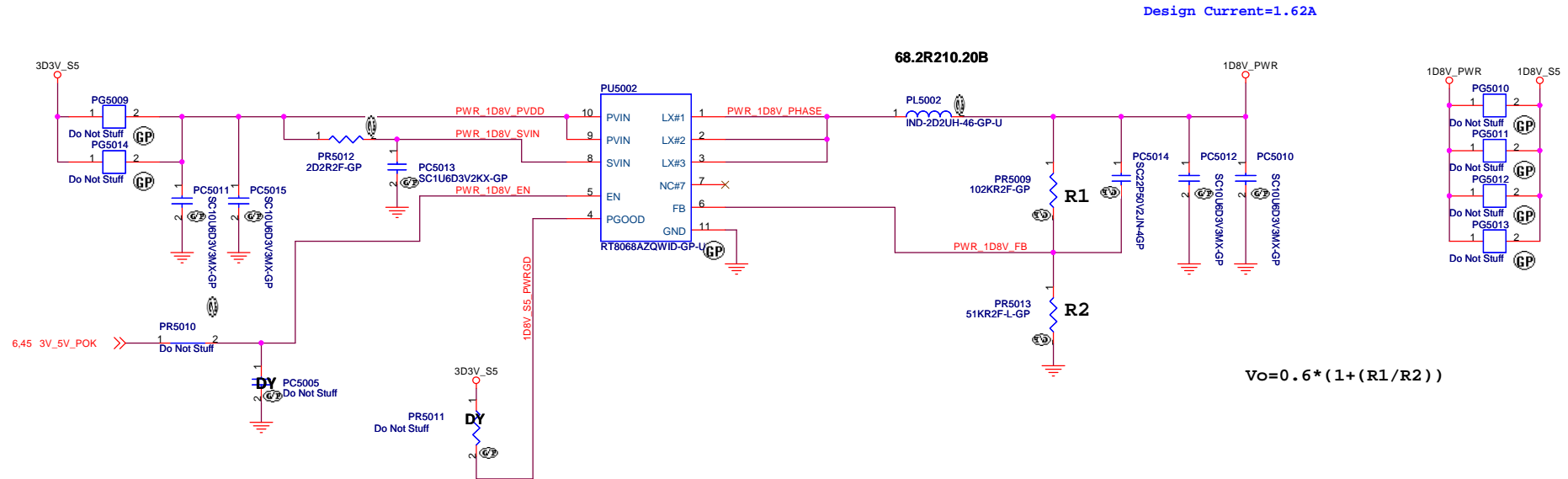
State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

```
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5-1.7mohm Isat =60Arms 68.R1010.10T
O/P cap: CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L
H/S:STS412 / 24.5mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:STS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037
```

TPS51716 MODE		
PR4608	Frequency	Discharge Mode
33k ohm	500kHz	Non-tracking Discharge
22k ohm	670kHz	
12k ohm	670kHz	Tracking Discharge
1k ohm	500kHz	

SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S5



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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

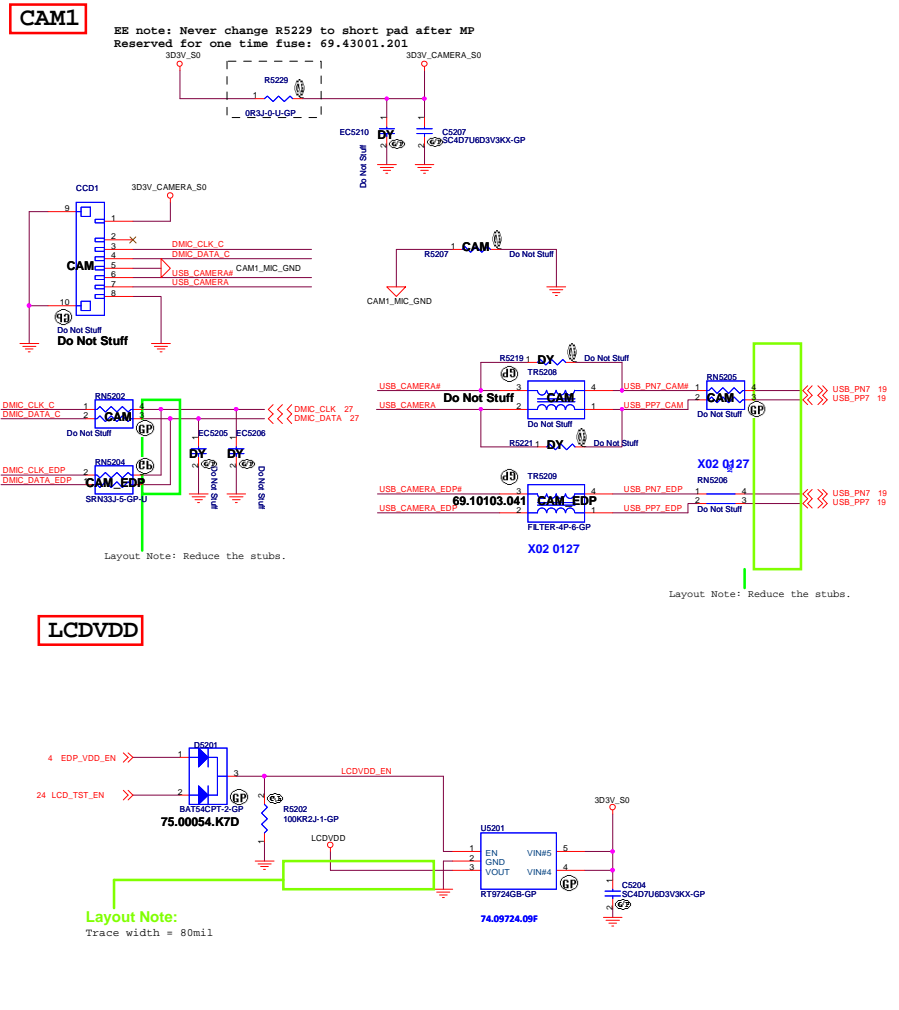
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Size	Document Number		Rev	
A3	Cedar AMD BEEMA		A00	
Date:	Wednesday, March 05, 2014		Sheet	50 of 104

SSID = PWR.Plane.Regulator_1p5v

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Cedar UMA 14

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title TLV70215_1D5		
Size A3	Document Number Cedar AMD BEEMA	Rev A00
Date: Wednesday, March 05, 2014	Sheet 51 of	104

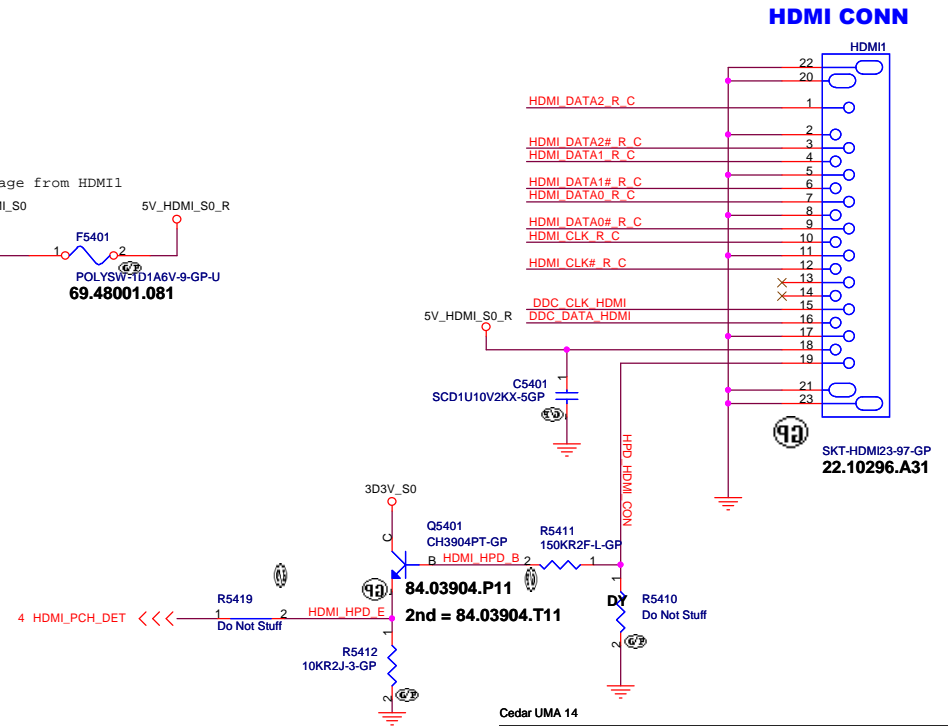
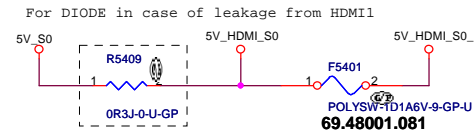
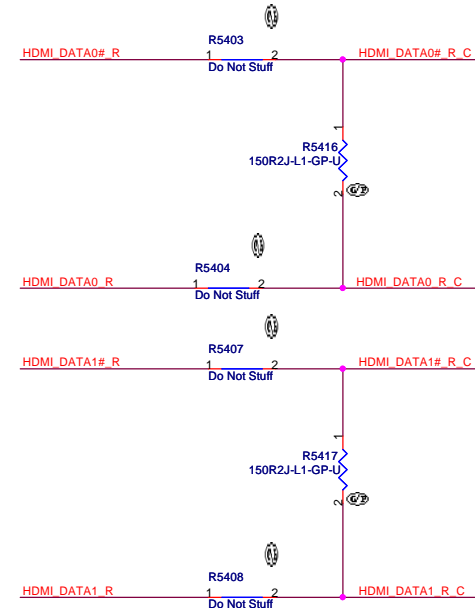
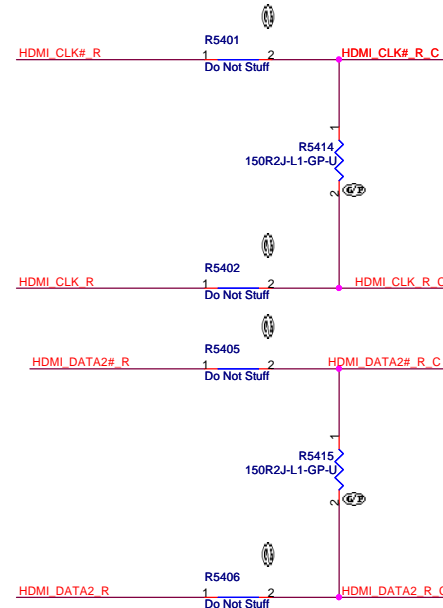
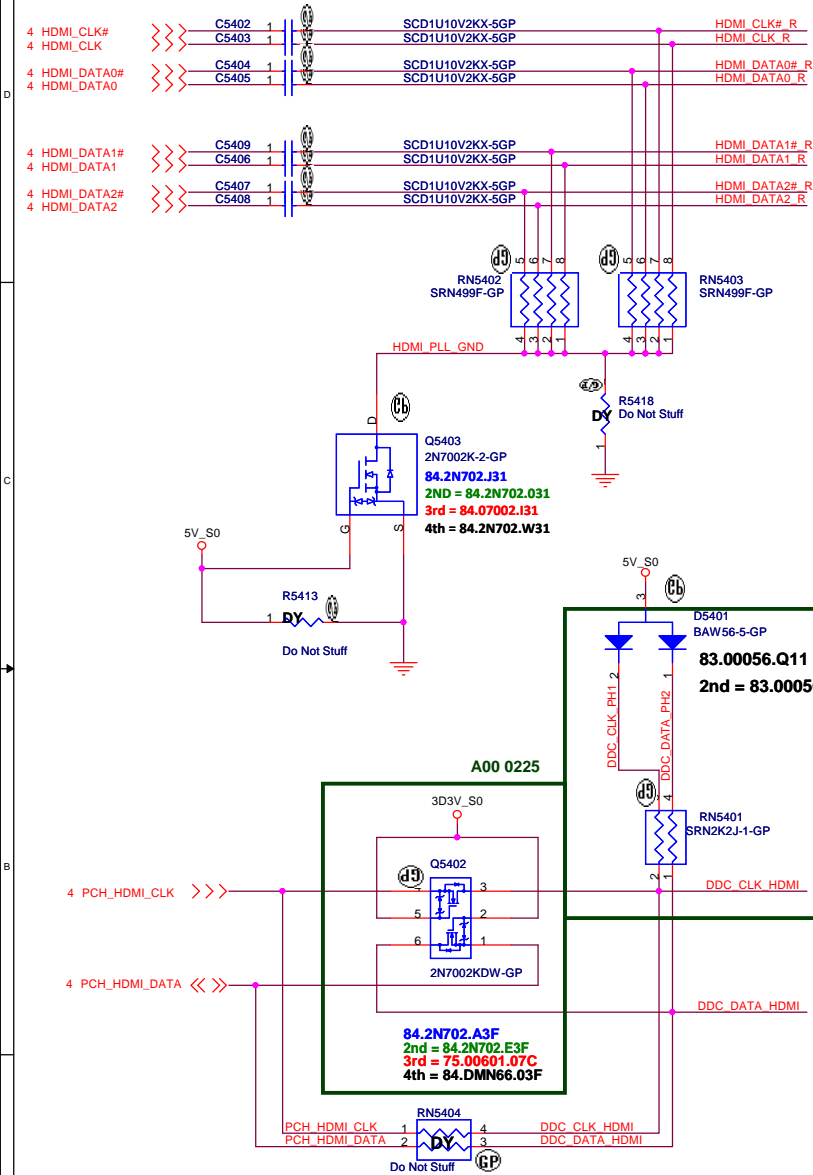


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緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserved)			
Size	Document Number		Rev
A3	Cedar AMD BEEMA		A00
Date: Wednesday, March 05, 2014		Sheet 53 of 104	

SSID = VIDEO



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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
A3		A00
Date:	Wednesday, March 05, 2014	Sheet 54 of 104

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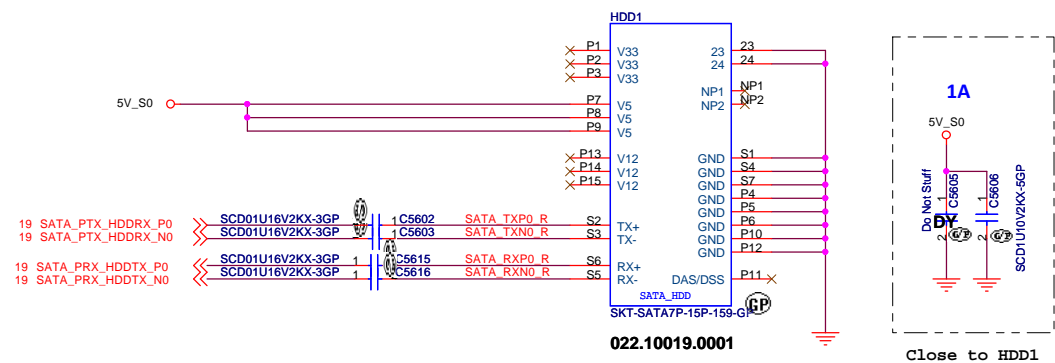
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Cedar UMA 14

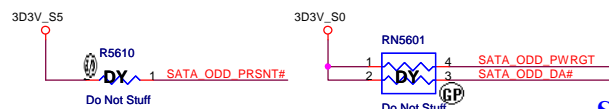
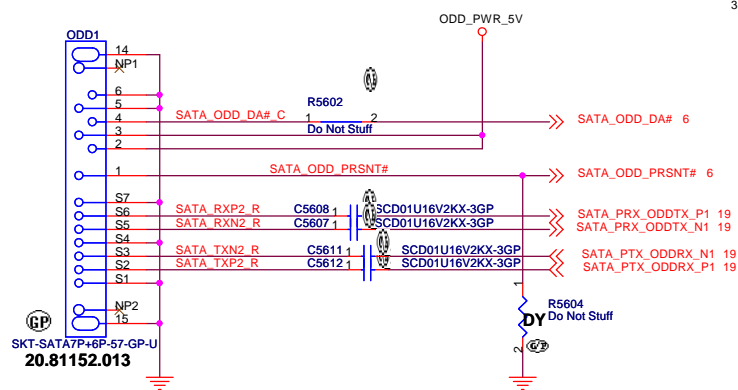
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<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>			
Title			
VGA Con.(Reserve)			
Size	Document Number		Rev
A3	Cedar AMD BEEMA		A00
Date: Wednesday, March 06, 2014		Sheet	55 of 104

SSID = SATA

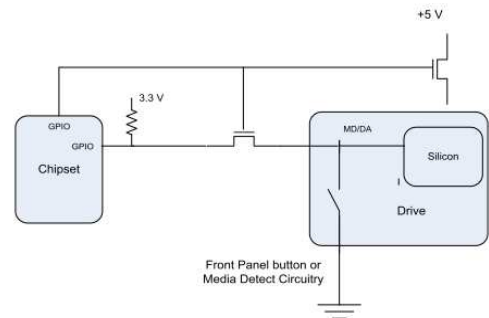
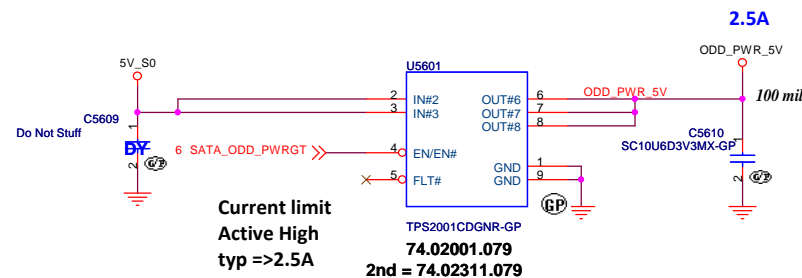
SATA HDD Connector



ODD Connector



SATA Zero Power ODD



SSID = ESATA

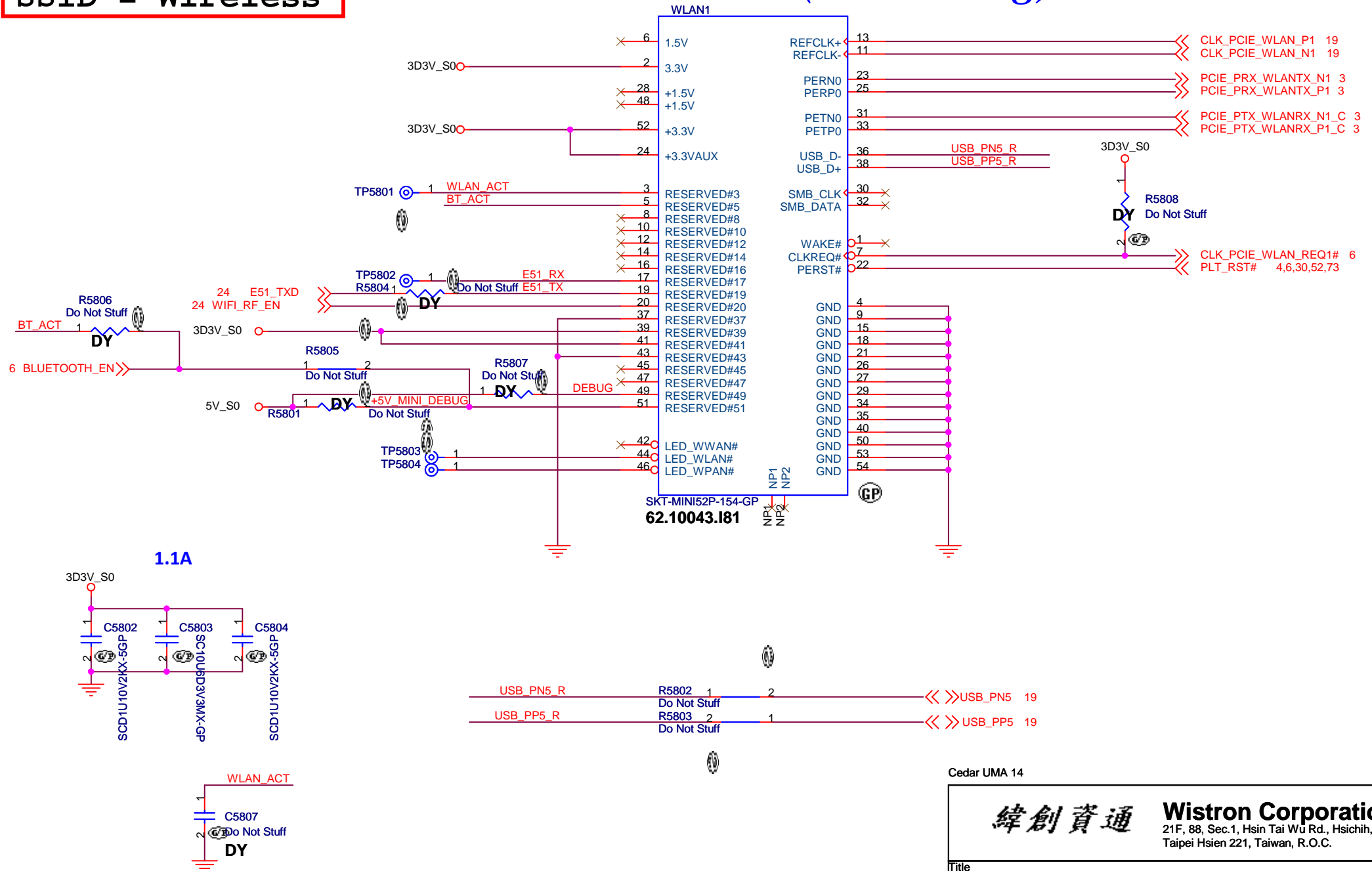
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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		ESATA	
Size	Document Number		Rev
A3	Cedar AMD BEEMA		A00
Date:	Wednesday, March 05, 2014	Sheet	57 of 104

SSID = Wireless

Mini Card Connector(802.11a/b/g)



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Cedar UMA 14

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

WLAN CONN

Size

A4

Document Number

Cedar AMD BEEMA

Rev

A00

Date: Wednesday, March 05, 2014

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Cedar UMA 14

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Reserved</i>			
Size A4	Document Number <i>Cedar AMD BEEMA</i>		Rev <i>A00</i>
Date:	Wednesday, March 05, 2014	Sheet 59 of	104

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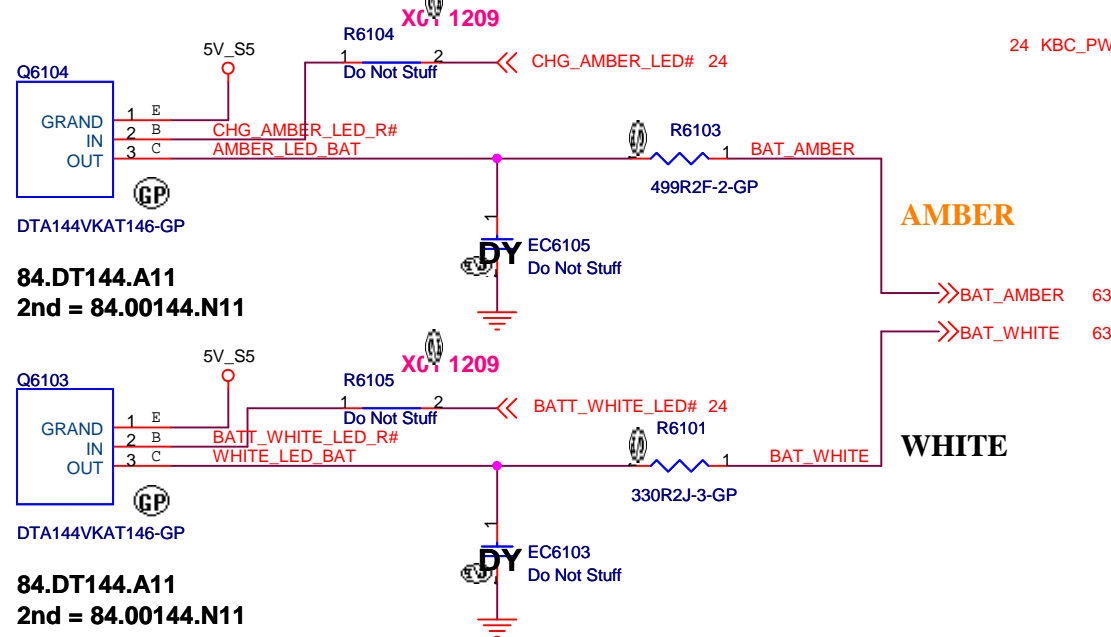
Cedar UMA 14

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div> <div>(Reserved)</div>			
<div>Size</div> <div>A4</div>	<div>Document Number</div> <div>Cedar AMD BEEMA</div>		<div>Rev</div> <div>A00</div>
<div>Date: Wednesday, March 05, 2014</div>		<div>Sheet</div> <div>60</div>	<div>of</div> <div>104</div>

SSID = User.Interface

Battery LED1 (AMBER_LED)

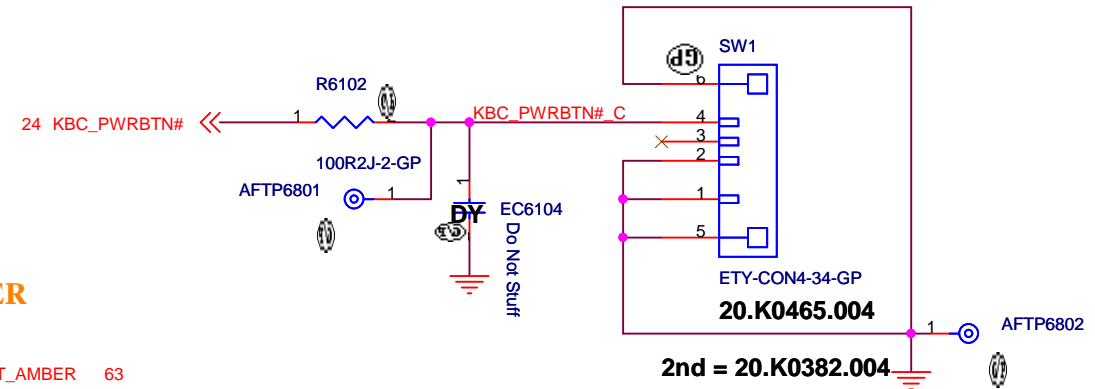
Low activated from KBC GPIO



Battery LED2 (WHITE_LED)

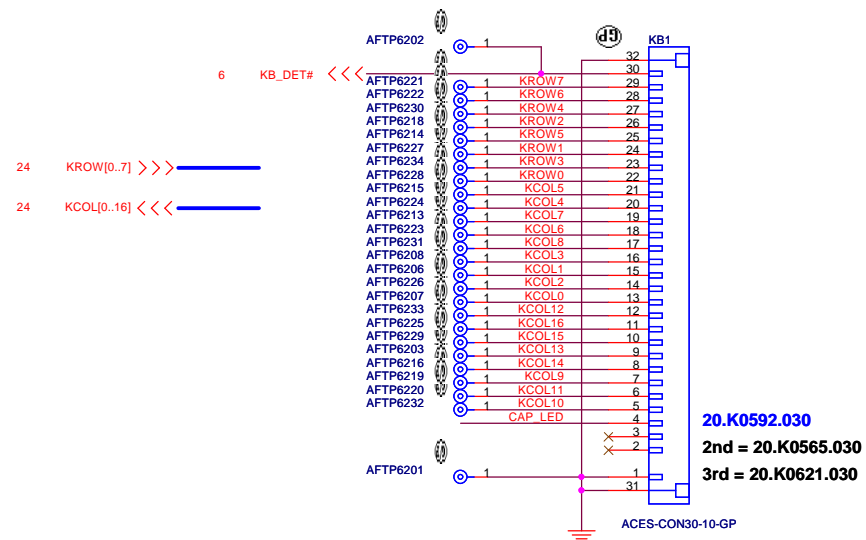
Low activated from KBC GPIO

Power button

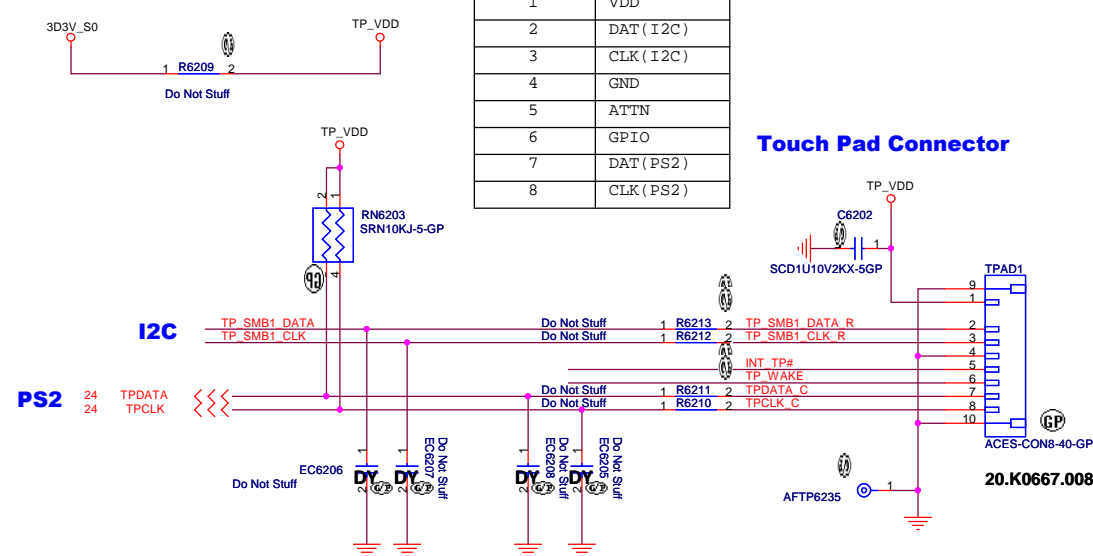


SSID = KBC

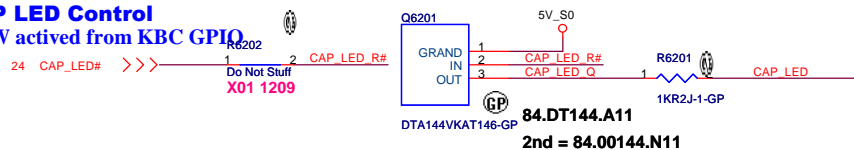
Internal Keyboard Connector (DVC40)



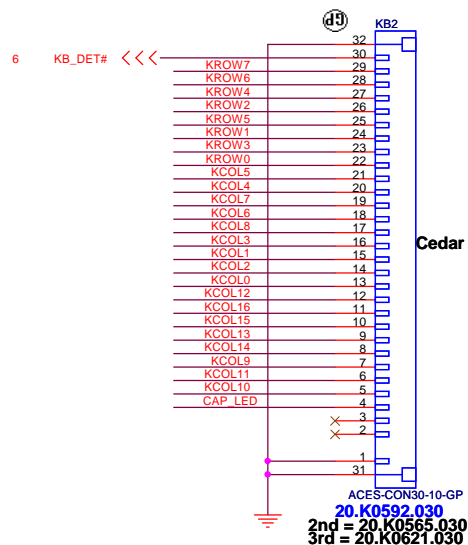
SSID = Touch.Pad



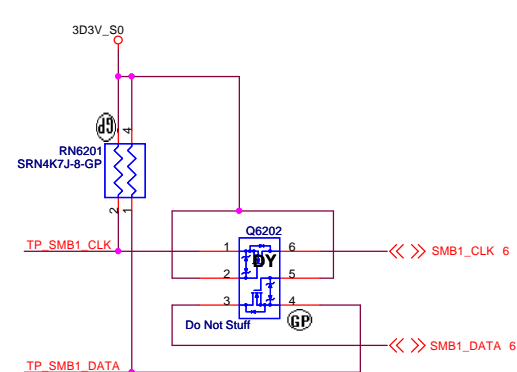
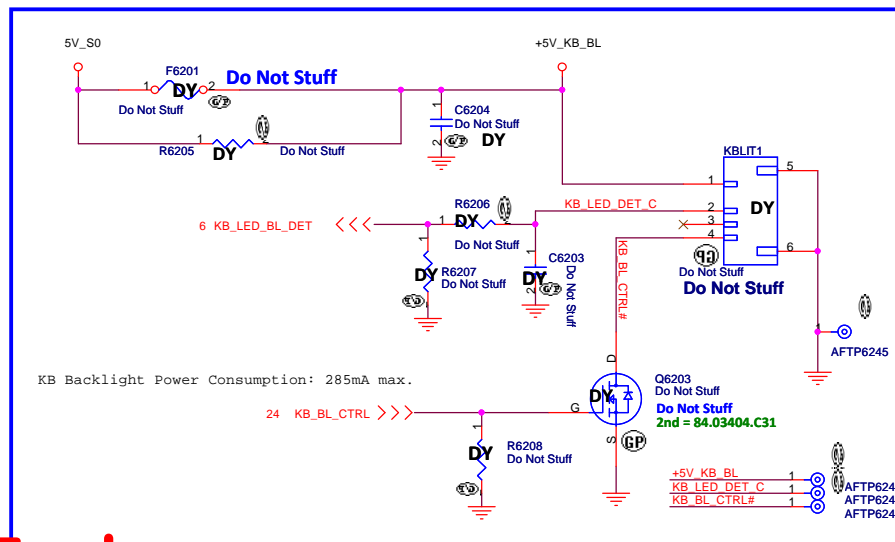
CAP LED Control LOW acted from KBC GPIO

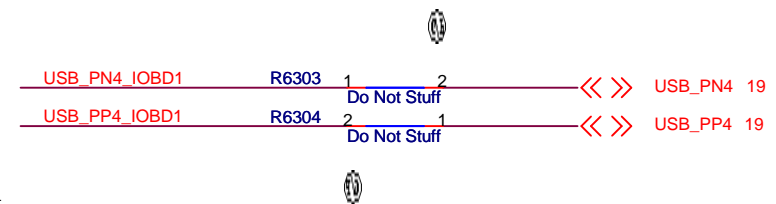
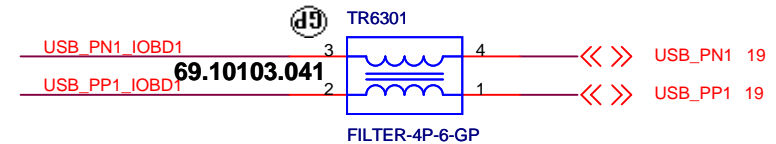
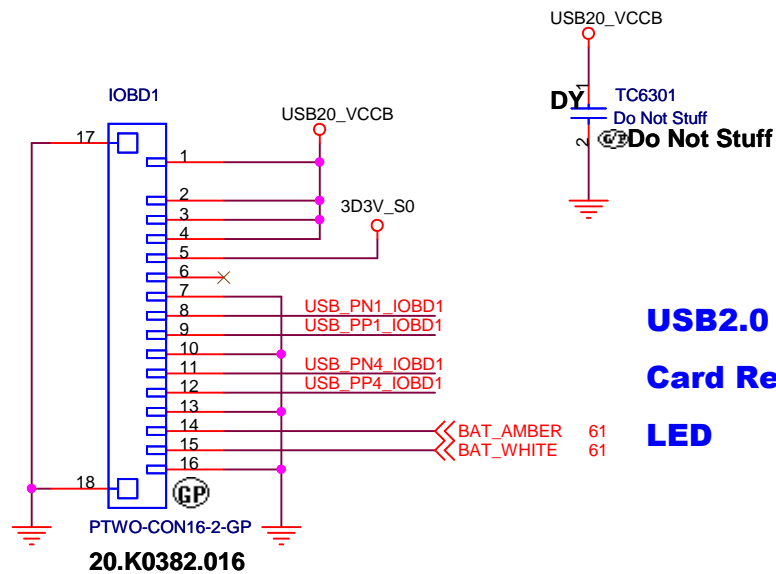


Internal Keyboard Connector (DVC50)



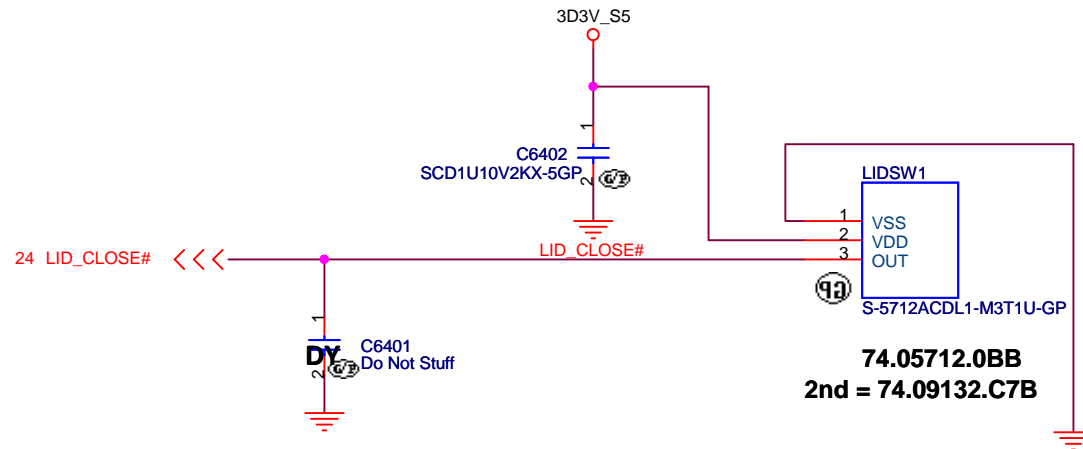
Keyboard Backlight





The maximum range of the PMOS output current in RTS5170 (Card Reader IC) is 400mA

SSID = User.Interface



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Title			
Hall Sensor			
Size A4	Document Number Cedar AMD BEEMA		Rev A00
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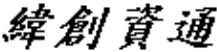
Cedar UMA 14

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Title			
<i>Reserved</i>			
Size A4	Document Number <i>Cedar AMD BEEMA</i>		Rev <i>A00</i>
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Title			
Thunderbolt (1/5)			
Size A4	Document Number		Rev
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Title <div>Thunderbolt (2/5)</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
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Title <div>Thunderbolt (3/5)</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
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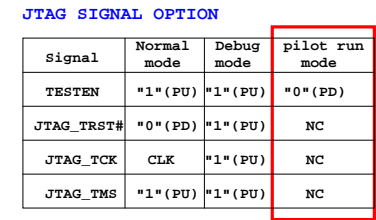
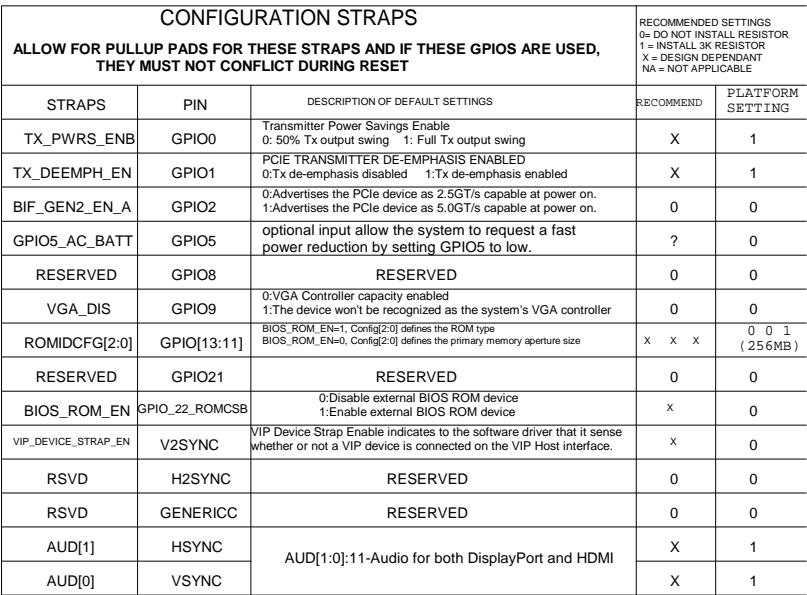
Cedar UMA 14

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Thunderbolt (4/5)</div>		
Size <div>A4</div>	Document Number <div>Cedar AMD BEEMA</div>	Rev <div>A00</div>
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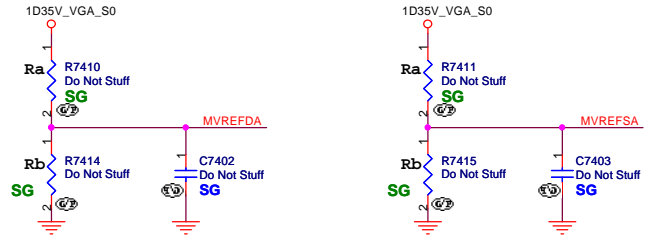
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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Thunderbolt (5/5)			
Size A4	Document Number Cedar AMD BEEMA		Rev A00
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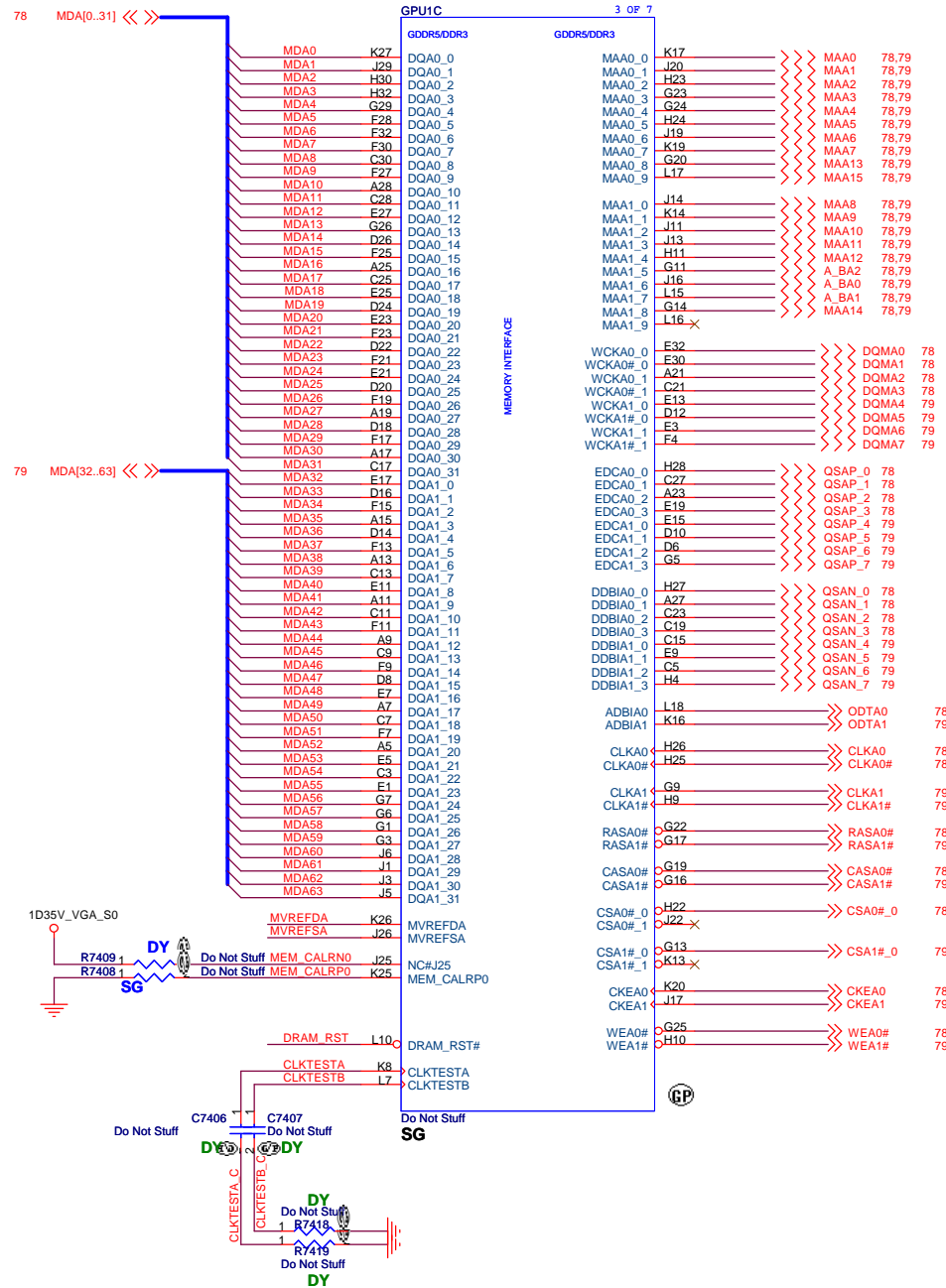
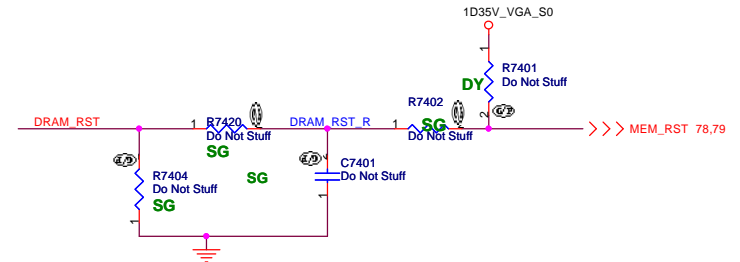


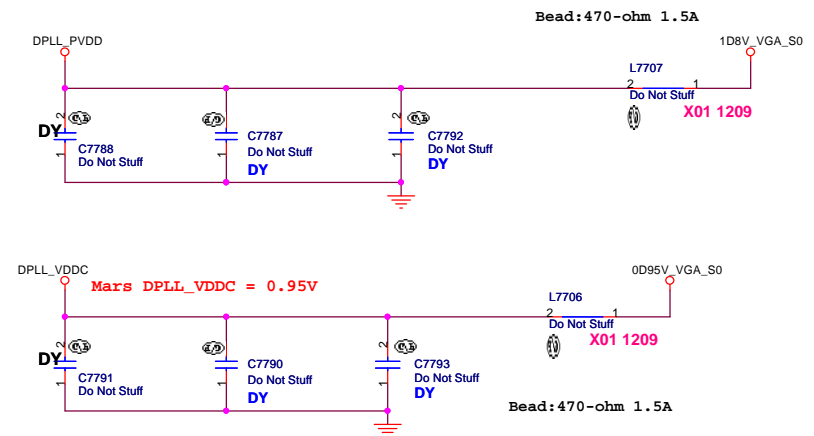
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

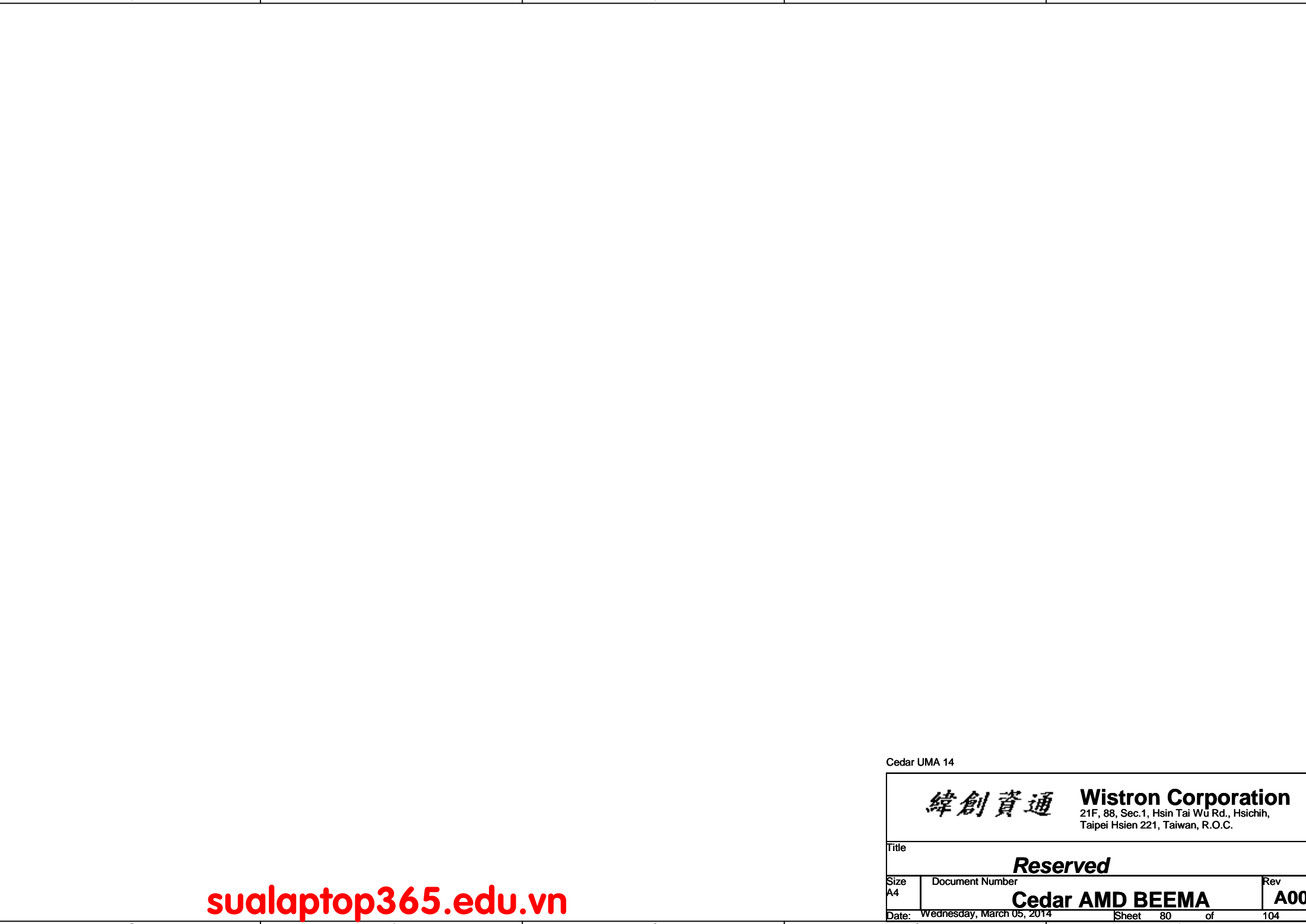


DDR3/GDDR3 Memory Stuff Option(Mad/Park)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1.8V/1.5V	1.35V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R







D

D

C

C

B

B

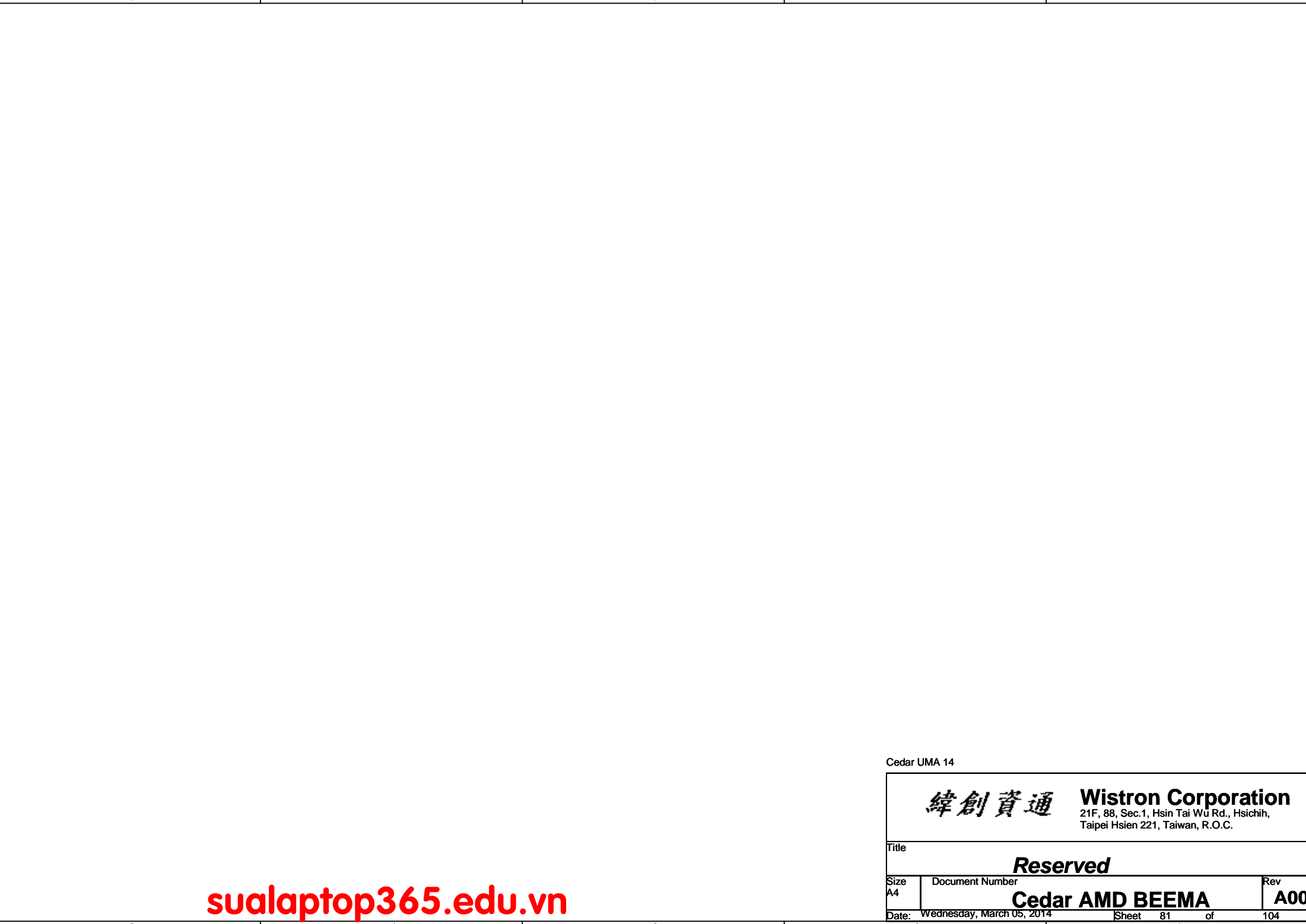
A

A

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D

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Pre-PWROK METAL VID CODES

SVD	SVC	Output Voltage
0	0	1.1
1	0	1.0
0	1	0.9
1	1	0.8

75 GPU_VGA_SVC >>>
75 GPU_VGA_SVD >>>
6.24.83 DGPI_PWROK <<<
24.75 GPUOTHER_ALERT# <<<

73 ATL_RST# >>>
2ND = 73.7S208.DAH

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKER 0.36UH PCME064T-R36MS1R407 1.4mohm / Isat =24Arms 68.R3610.20W
O/P cap:CHIP CAP 470UF 2V BEFSX0D471X /Panasonic/ 6mOhm / 79.47719.2BL
CHIP CAP EL 330U 2.5V M6.3*4.4 3.5Arms Chemi-con/79.3371V.6CL
FET MOSFET: SIRA14DP / 6.8mohm/ 8.5mohm / 2.9mOhm/ 3.5mohm@4.5Vgs / 84.A14DP.037
/S: 1.4mohm/ 8.5mohm / 2.75mOhm/ 3.5mohm@4.5Vgs / 84.SRA06.037

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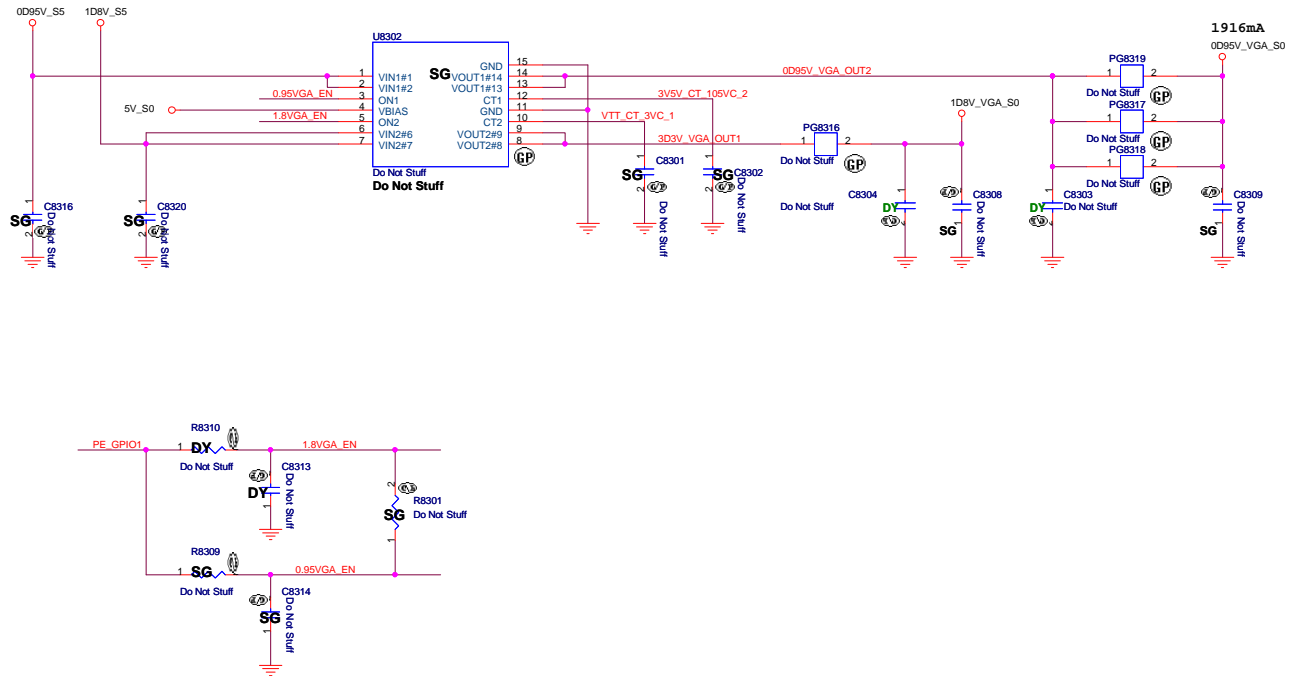
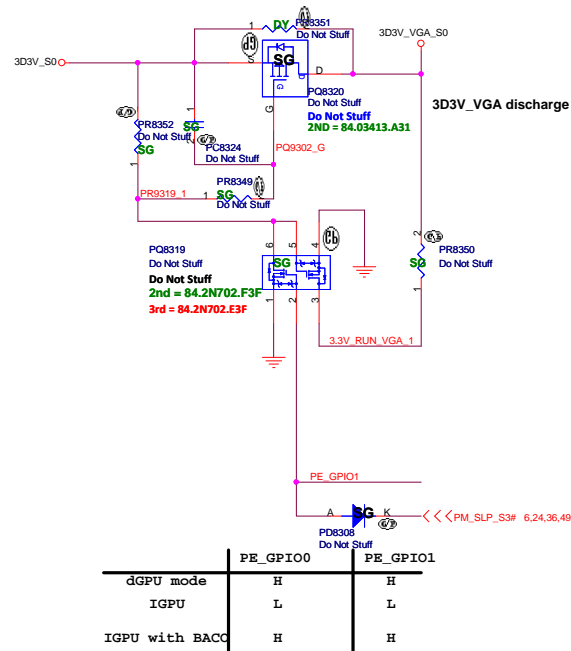
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsueh,
Taipei Hsien 221, Taiwan, R.O.C.

RT8179A VGACORE		
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3D3V_S0 to 3D3V_VGA_S0 Transfer

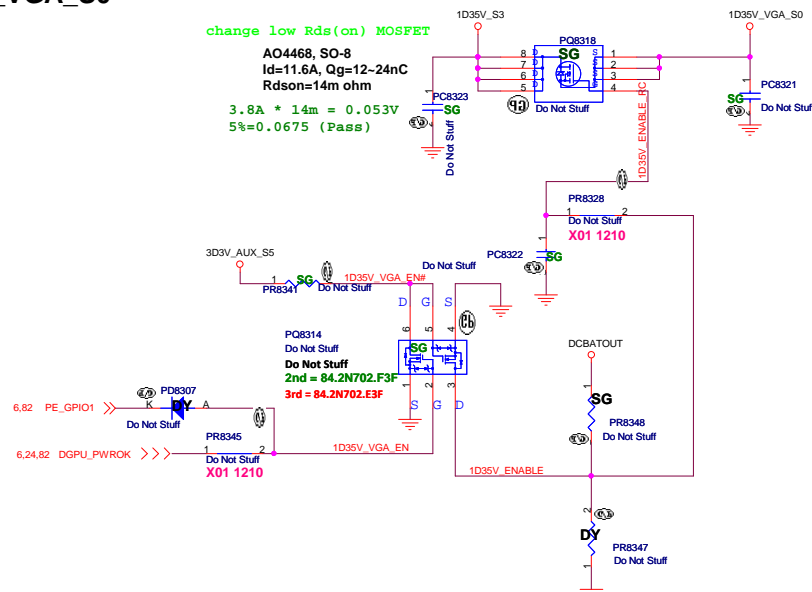
Change DUMMY Reference Name to PX_BACO



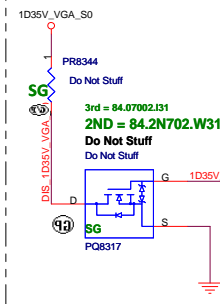
finally rising of 1.8_VGA_S0

1D5V_VGA_S0

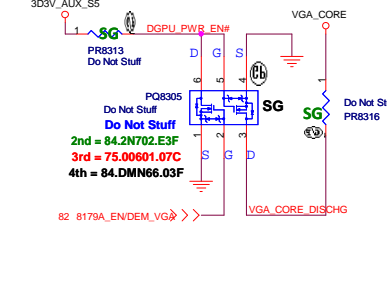
change low $R_{ds(on)}$ MOSFET
 AO4468, SO-8
 $I_d=11.6A$, $Q_g=12-24nC$
 $R_{ds(on)}=14m\ ohm$
 $3.8A * 14m = 0.053V$
 $5\% = 0.0675$ (Pass)



Discharge Circuit



VGA_CORE Discharge Circuit



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Title			
DISCRETE VGA POWER			
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Custom		A00	
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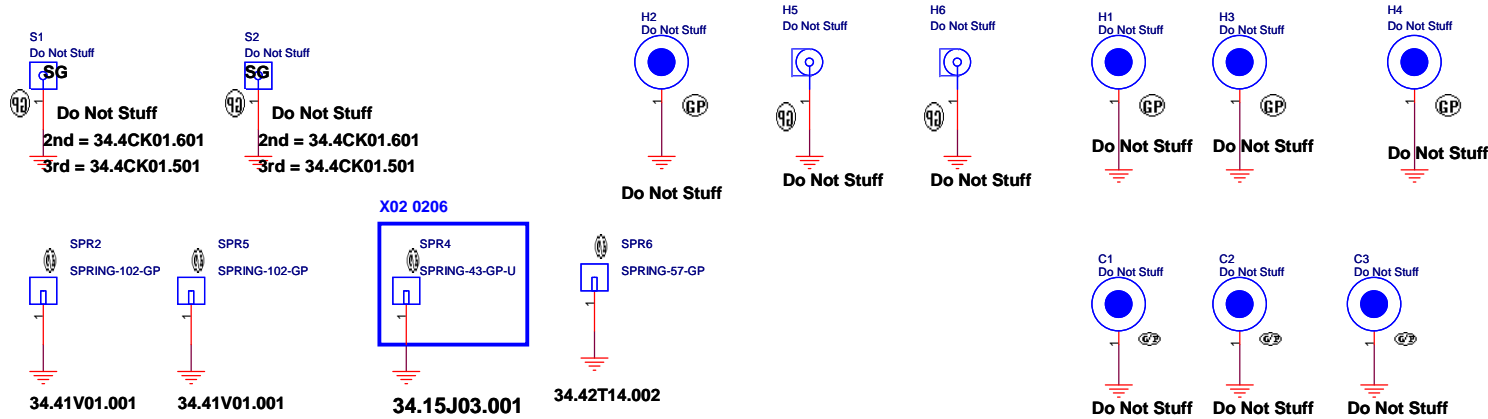
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>(Reserved)</div>	
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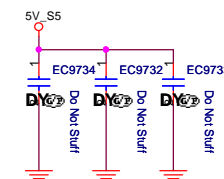
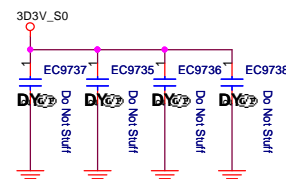
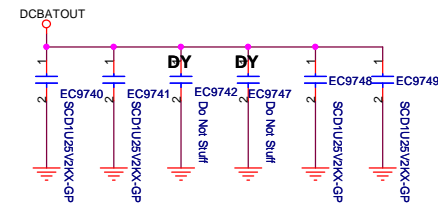
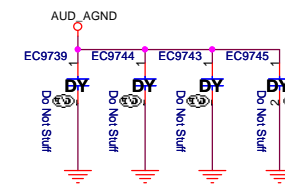
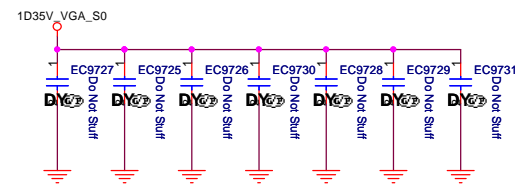
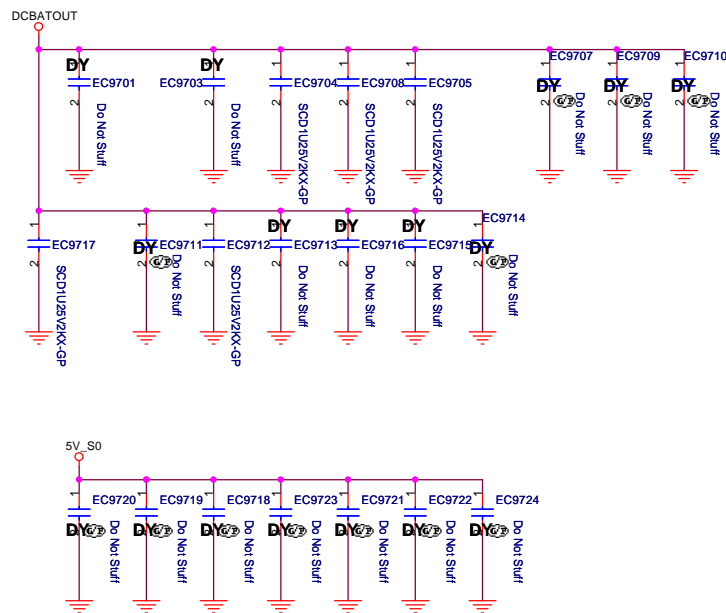
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Title <div>(Reserved)</div>		
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SSID = Mechanical




SSID = EMI



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NFC(Reserved)			
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File			
TEST PAD			
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Title <div>(Reserved)</div>	
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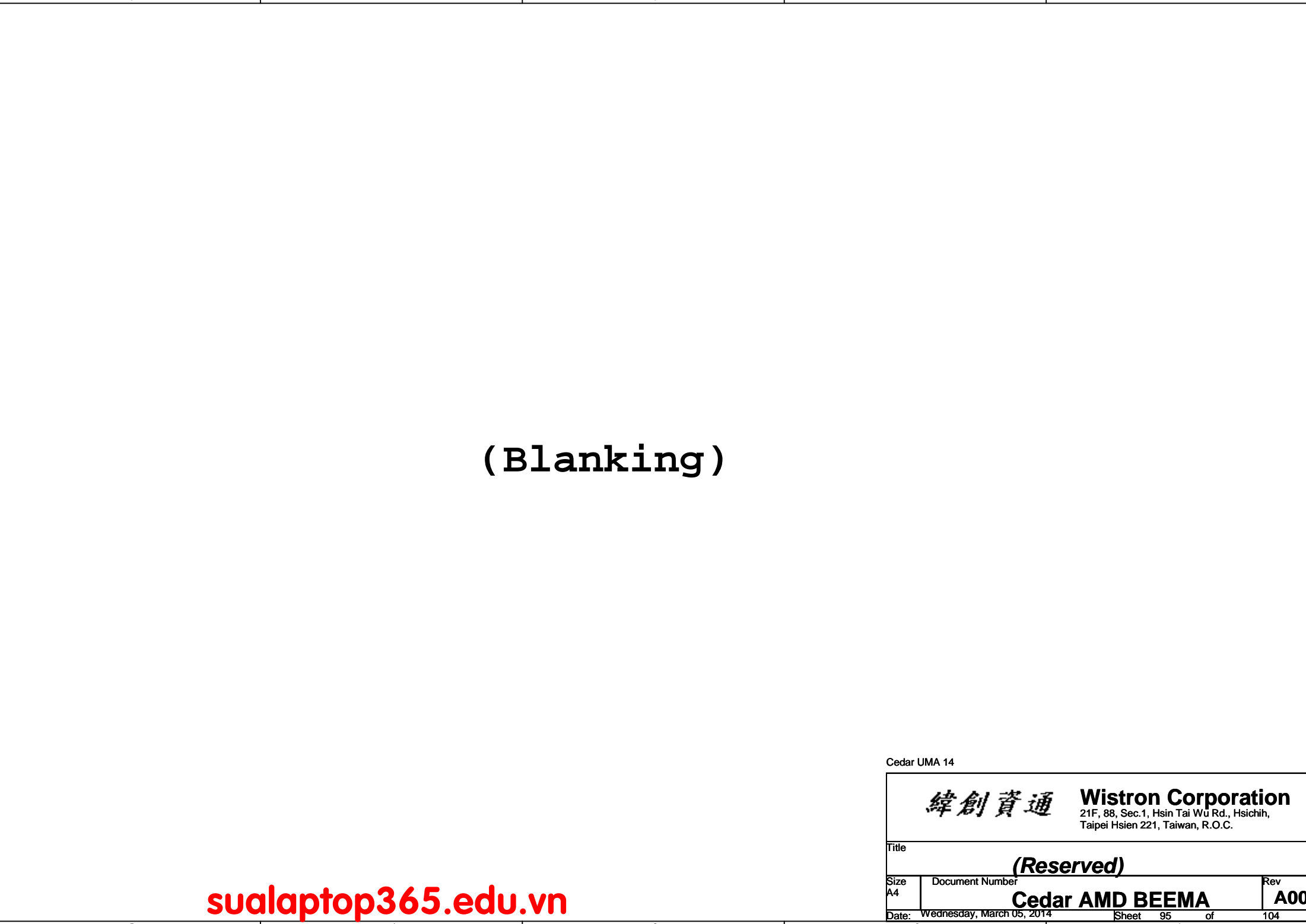
Cedar UMA 14

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title <div>(Reserved)</div>	
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Title <div>(Reserved)</div>	
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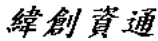
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Title			
MCP CPU XDP HDT+			
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Title		
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Wistron Corporation

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Title

Change History

Size
A3

Document Number
Cedar AMD BEEMA

Rev
A00

Date: Wednesday, March 05, 2014

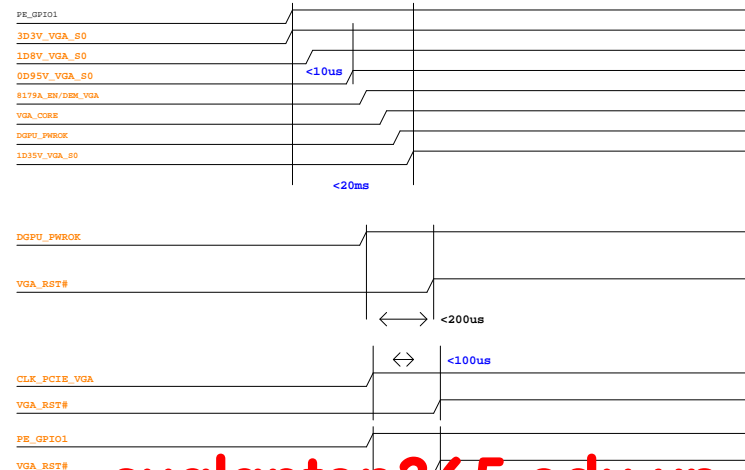
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red word: KBC GPIO

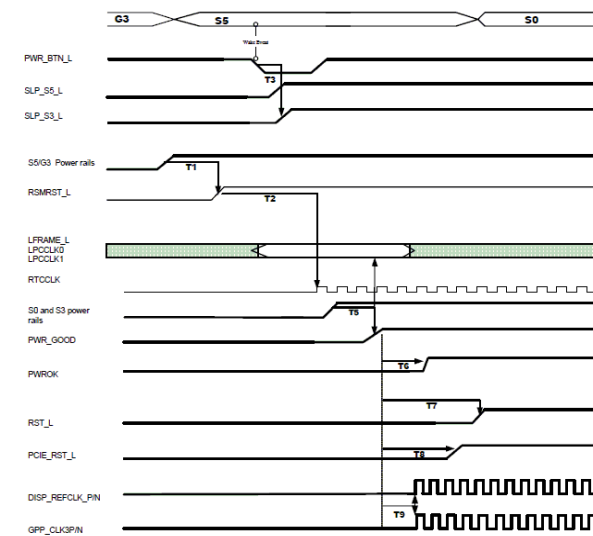
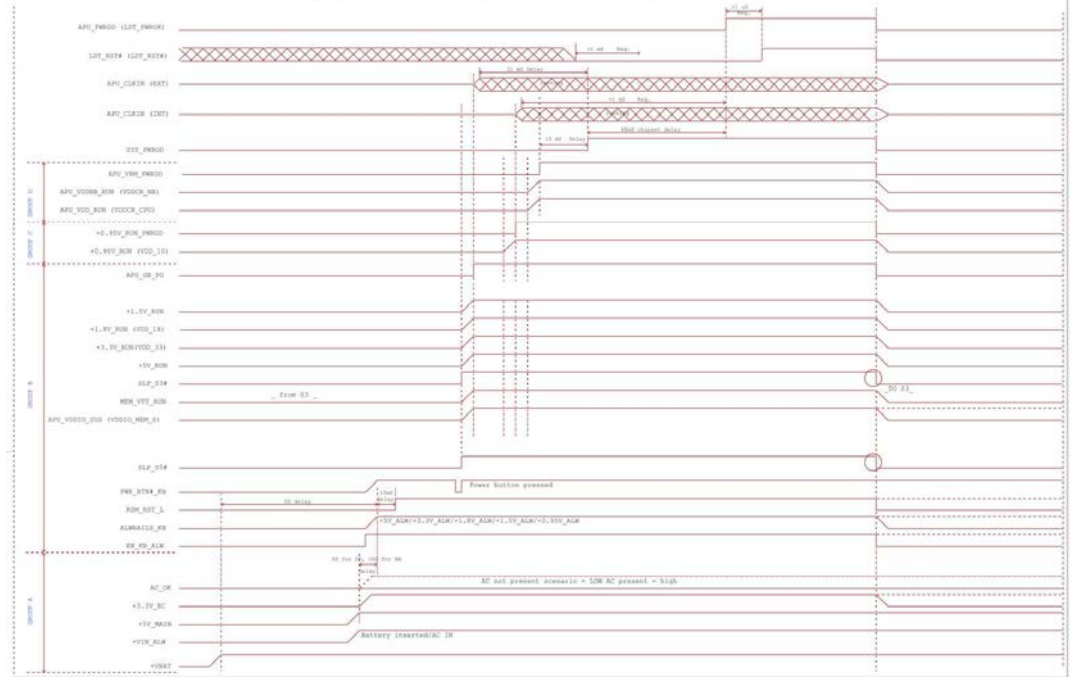
Within logic high level and disable if it is less than the logic low level.

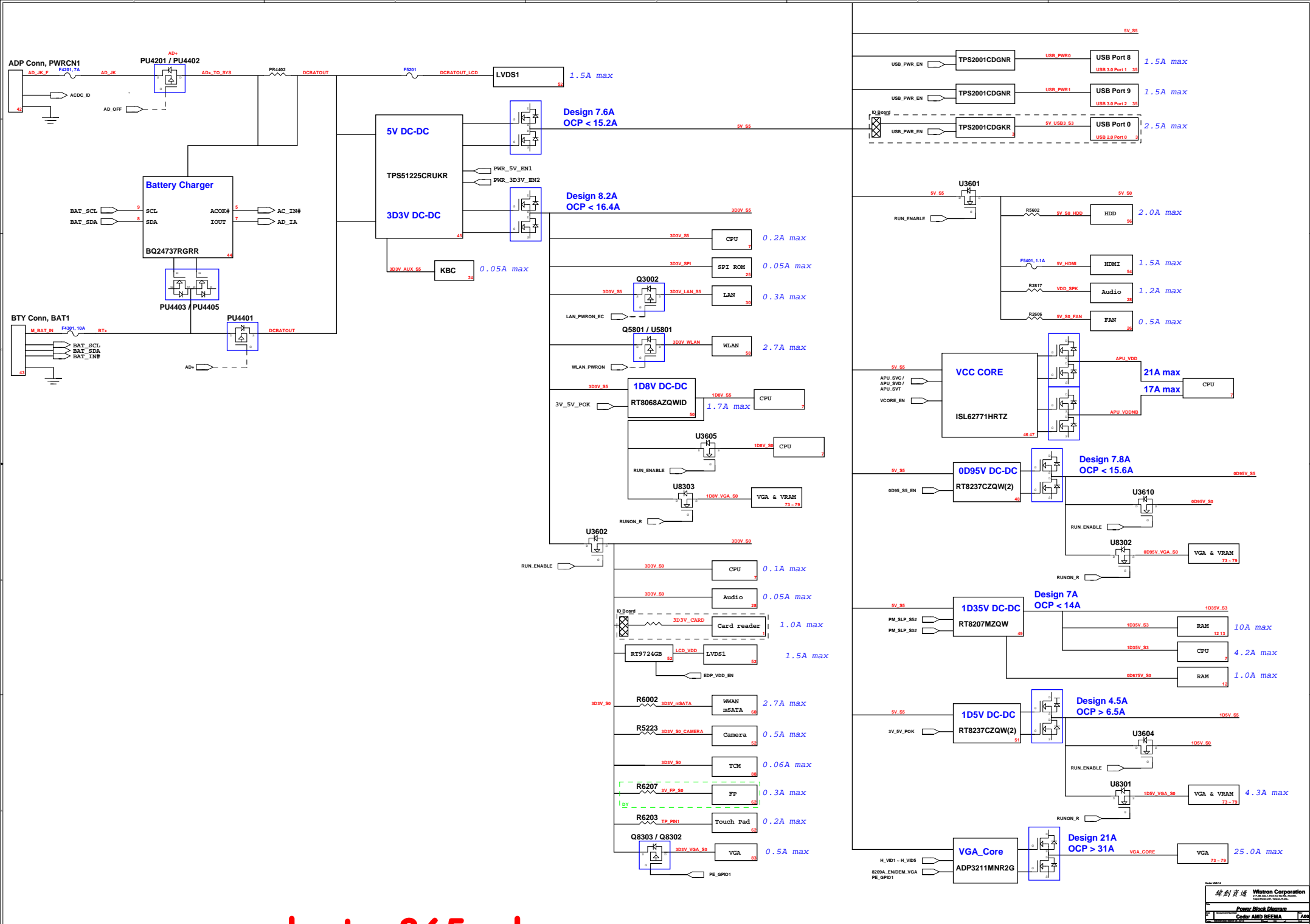
Ta

VREF_Bus must be powered up before VccHdual_1, or after VccHdual_1 within 0.7 V. Also, VREF_Bus must power down after VccHdual_1, or before VccHdual_1 within 0.7 V.

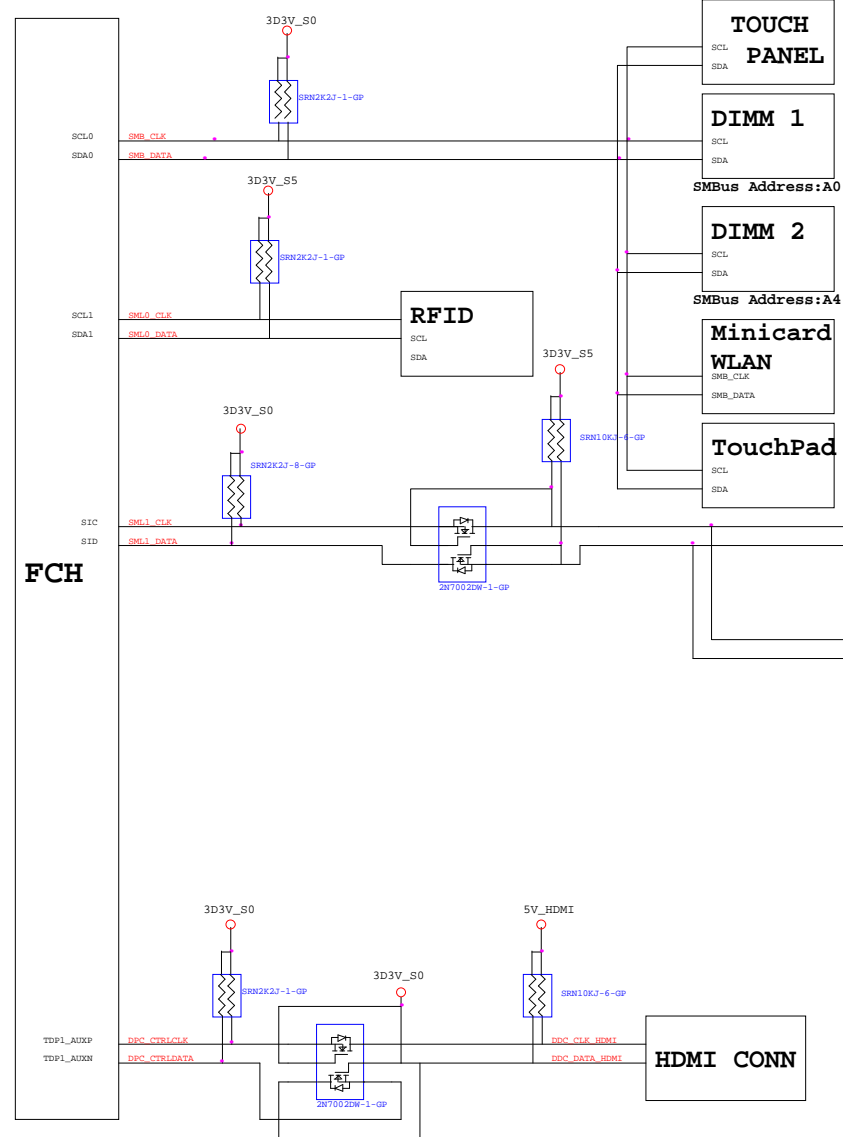


Power-up Sequencing for the KABINI Platform from Mechanical Off

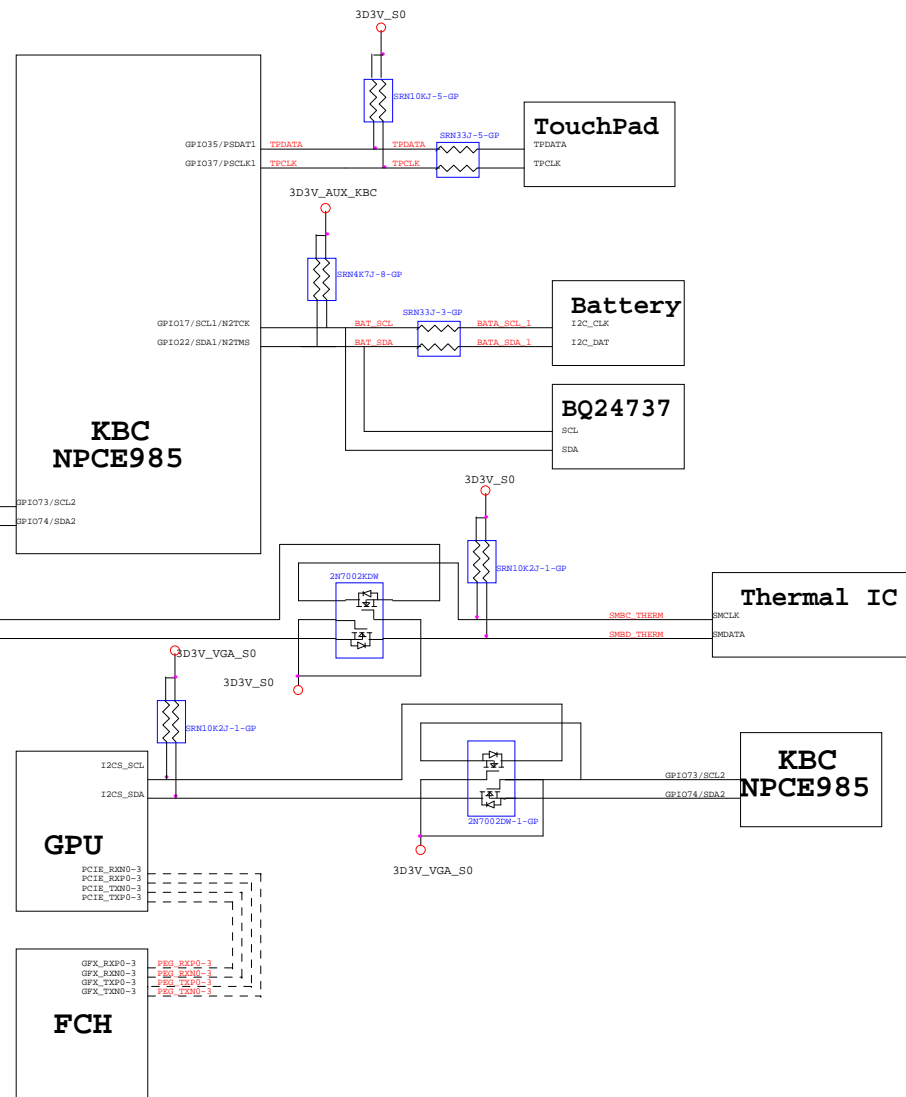




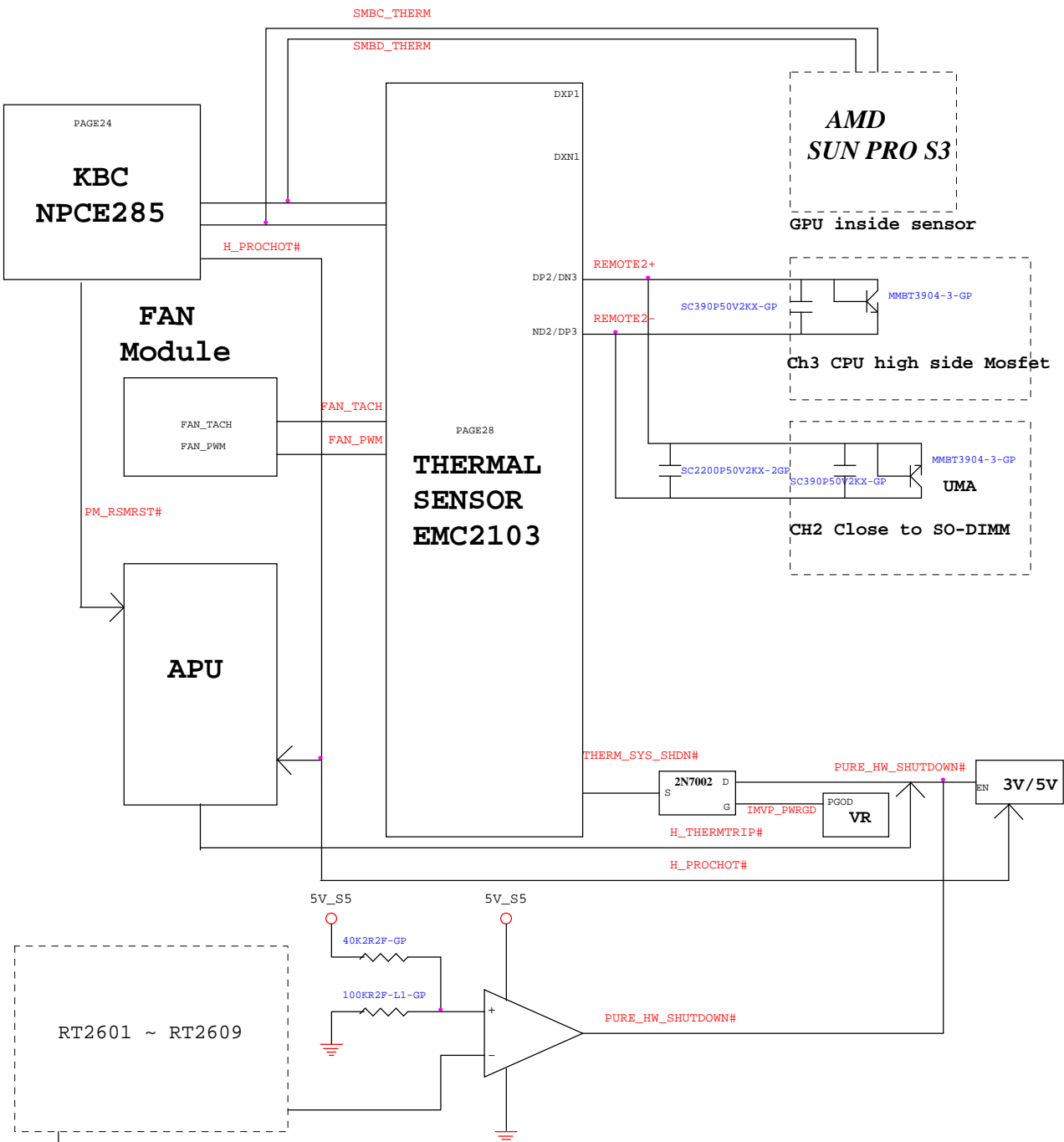
PCH SMBus Block Diagram



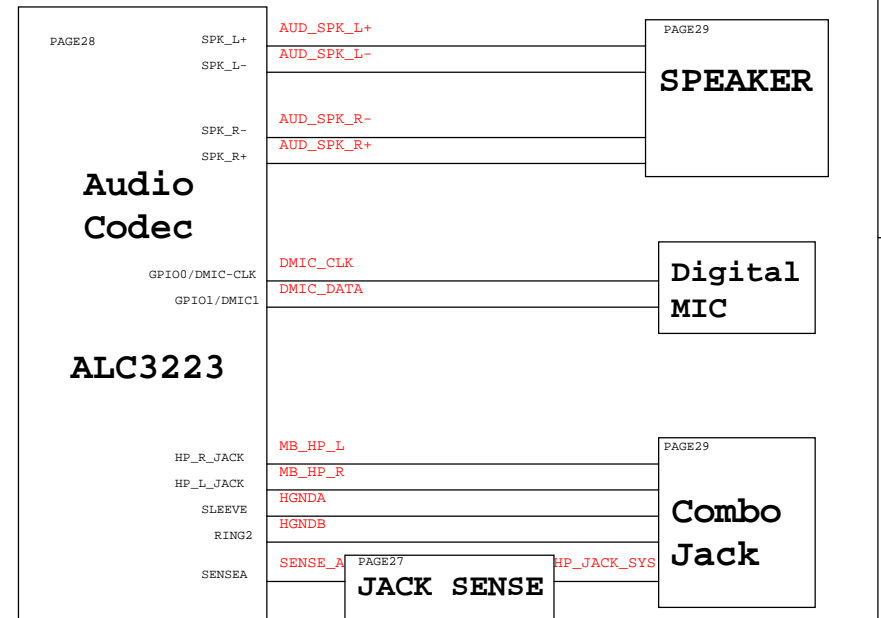
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Change notes -

	VERSION	DATE	Page	Modify List	OWNER
	X01	2013/12/3	83	R8309 = 15Kohm ,C8301/C8313 = DY,C8302 = 1000pF	
	X01	2013/12/3	43 44	RN4301 to 100ohm, AC_IN# change to Pull-H 3D3V_AUX_S5(PR4434)	
	X01	2013/12/3	27	HDA27 change from ALS3223 to ALC3234	
	X01	2013/12/3	24 25	Swap BATT_WHITE_LED# and EC_BRIGHTNESS. BATT_WHITE_LED# to GPIO13 and EC_BRIGHTNESS to GPIO15. Change R2404 from 10K to 20K ohm for PCB VERSION strap , Del SKT25	
	X01	2013/12/3	52	Reserve 0805 0 ohm R5211 between LCDVDD and LCD1.F5201 change from 69.50007.A31 to 69.60040.001	
	X01	2013/12/3	Power	Change C5205,EC4304,EC4601,PC4409,PC4419,PC4511.PC4518,PC4524,PC4720,PC4722,PC4827, PC4913 to 78.10422.2BL (0.1U 25V K0603 X7R) from 78.10424.2BL (0.1U 50V K0603 X7R).	
	X01	2013/12/3	54 55	Add HDMI SMBUS use 0 ohm DUMMY co-lay ,Add Hsync Vsync 0ohm DUMMY co-lay	
	X01	2013/12/3	29	Change HPMIC1 to 022.10002.0001 from 22.10270.G61 SPK1 change to 20.F1639.004	
	X01	2013/12/3	34 63	Change USB1 to 22.10341.Q21 / Change KBLIT1 to 20.K0800.004	
	X01	2013/12/3	19 26	Change C1904 and C1905 from 10pf to 6.8pf / Q2601 RN2602 DUMMY, RN2601 install	
	X01	2013/12/3	30	R3004 CLK_LAN_REQ0#_R change pull high to 3D3V_S0	
	X01	2013/12/3	EMI	DMIC_CLK mount R2716 100ohm resistance,Mount EC9749,Mount EC4304	
	X01	2013/12/3	58	CARD_WLAN_OUT# and CARD_WPAN_OUT# modify to TP change WLAN1 to 62.10043.I81	
	X01	2013/12/3	42 51	DCIN1 change to 20.F1783.007,Del 1D5V_S5 circuit	
	X01	2013/12/4	24 34 35	R2447 change to 63.10334.1DL,Del U3502 and U3501,swap the net U3403.1 and U3403.3	
	X01	2013/12/5	42 46 24 26	Del AFTP3804 AFTP3807, Modify AFTP6241 Add AFTP6242,Change R2447 to 1K , R2622 change to 24.3K	
	X01	2013/12/6	24	R2411 DY D2401 install	
	X01	2013/12/9	31 47 82	RJ45 connector change to 022.10001.0551, PT4701 /PT4704/PT8204 change to 79.3371V.6CL	
	X01	2013/12/10	EMI	Mount EC4303 and change to 0.1u Mount EC9705 EC9748 EC9717 EC9740 EC9741 EC9712 EC9704 EC9708 and change to 0.1u Mount R5415、R5417、R5416、R5414 150ohm resistance Mount TR3401、TR3404、TR6301(69.10103.041、69.10080.011) Mount TR5208、TR5209(69.10103.041、69.10080.011) Mount EC2705、EC2703、EC9739、EC9743、EC9744 0.1u cap Mount SPR2、SPR5、SPR6	
	X01	2013/12/10	0 ohm	change 0 ohm to short pad	
	X01	2013/12/10	54 55	R5501/R5502 change to 33 ohm / Del D5402	
	X01	2013/12/10	24 52 62	R2411 Install D2401 DUMMY ,R5207 BOM control ,BOM control DVC50 to Janus	
	X01	2013/12/12	46 86 62	PR4609 change to 44.2K (64.44225.6DL) from short pad, EMI:Add SPR6(34.42T14.002),KBLIT DUMMY	
	X01	2013/12/16	55 Power	Del CRT circuit / Modify power schematic BOM	
	X01	2013/12/18	Power	PR8214 change to 499K (64.49935.6DL) / PR8215 change to 9.76K (64.97615.6DL)	

Cedar UMA 14

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Title

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	VERSION	DATE	Page	Modify List	OWNER
	X02	2014/01/21	48	Change PR4823 to 26.1K. The voltage about 0.97V	
	X02	2014/01/21	83	R8310 change 15Kohm /C8313 change 0.1uF /C8301 change 470pF Add R8301 for power sequence	
	X02	2014/01/27	12,46	EMC request:change EC4601,C1217,C1225,C1214 to 0.1u	
	X02	2014/01/27		Change 0 ohm to short pad	
	X02	2014/01/27	6	DGPU_PRESENT# pull hi to 3D3V_S0	
	X02	2014/01/28	power	1. PD4201 change 1st source to 83.P6SBM.AAG and 2nd source to 83.P6SBM.DAG . 2. PC4202 PC4409 PC4419 PC4519 PC4524 PC4511 PC4513 PC4518 PC4734 PC4720 PC4722 PC4736 PC4833 PC4827 PC4919 PC4913 3. PC4201 change to 78.10594.41L. 4. PC4916,PC4917 change to 78.10610.5BL. 5. PC4408 change to 78.47522.51L (4.7U 25V K0805 X5R). 6. PC4425 change to 78.10324.2FL (0.01U 50V K0402 X7R). 7. PC4512 change to 78.47522.51L (4.7U 25V K0805 X5R). 8. Delete PC4814/PC4714. 9. Dummy PC4718/PC4912/PC4920/PC4204/PC4205/ PC4426/PC4416/PC4830 10.PC4828 change to 78.47522.51L (4.7U 25V K0805 X5R). 11.PC4909 and PC4911 change to 78.47522.51L (4.7U 25V K0805 X5R).	PC8230
	X02	2014/01/28	31	change XF3101 and XF3102 to 68.68167.30D and Swap net	
	X02	2014/02/06	06 19	Change RN1901 R1901 from short pad to 0 ohm Change RN604 to 66.10336.08L	
	X02	2014/02/06	86	Change SPR4 P/N to 34.15J03.001	
	X02	2014/02/07	26	THM26 DUMMY, Add R2602 for VD_OUT1# connect PURE_HW_SHUTDOWN#	
	A00	2014/02/25		Change PR4911 PR4649 R3016 R6209 R1901 RN5404 RN1901 to short pad	
	A00	2014/02/25	82	Modify schematic PWR_VGA_COMP connecte to PWR_VGA_FB	
	A00	2014/02/25	24	PCB VERSION A/D(PIN98) R2404 change to 64.64925.6DL	
	A00	2014/02/25	54	Install D5401 RN5401 Q5402, Dummy RN5404	